ITS EINAUDI

Elettronica e Telecomunicazioni

Tecnologia e Disegno per la Progettazione Elettronica

Porte Logiche

PORTE LOGICHE - i parametri dei fogli tecnici

SGS-THOMSON MICROELECTRONICS

M54HC00
M74HC00

QUAD 2-INPUT NAND GATE

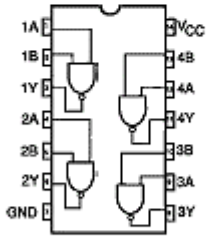
- HIGH SPEED
  t_{PD} = 6 ns (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 1 µA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
  V_{NH} = V_{NL} = 28 % V_{CC} (MIN.)
- OUTPUTS DRIVE CAPABILITY
  10 LSTTL LOADS
- BALANCED PROPAGATION DELAYS
  t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
  V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS00
- SYMMETRICAL OUTPUT IMPEDANCE
  $|I_{OH}|$ = I_{OL} = 4 mA (MIN.)

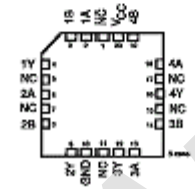
B1R (Plastic Package) F1R (Ceramic Package)
M1R (Micro Package) C1R (Chip Carrier)

ORDER CODES :

M54HC00F1R	M74HC00M1R
M74HC00B1R	M74HC00C1R

PIN CONNECTIONS (top view)



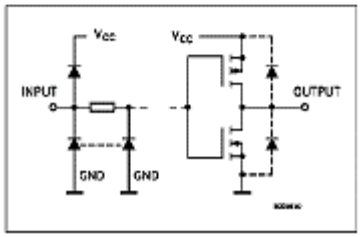


NC = No Internal Connection

DESCRIPTION

The M54/74HC00 is a high speed CMOS QUAD 2-INPUT NAND GATE fabricated in silicon gate C^2MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



December 1992 1/9

Valori Massimi Assoluti

Vcc max, Vin max, T max

Condizioni Operative Consigliate

Vcc - tolleranza %

Vin - V_{IH} – V_{IL}

T_A

Iout – I_{OH} – I_{OL}

(tf, tr)in

Caratteristiche Elettriche (Statiche)

V_{IH}, V_{IL}

V_{OH}, V_{OL}

I_{IH}, I_{IL}

I_{OSC}

I_{CC}

Symbol	Parameter	C_L = 15 pF	C_L = 50 pF	Units

Caratteristiche in Commutazione (Dinamiche)

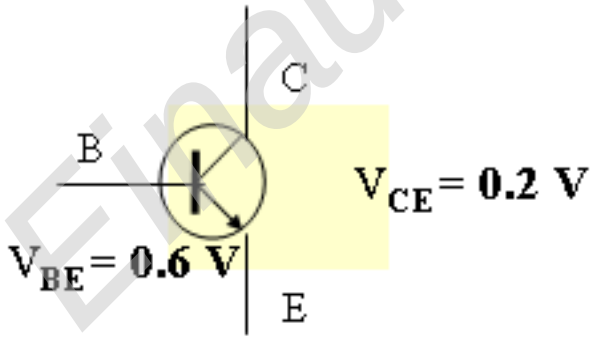
(tf, tr)out - T_{pHL}, T_{pLH}

Cin, Cpd

www.fairchildsemi.com 2

Approssimazione sui transistor usati nei circuiti digitali

Transistor Saturo

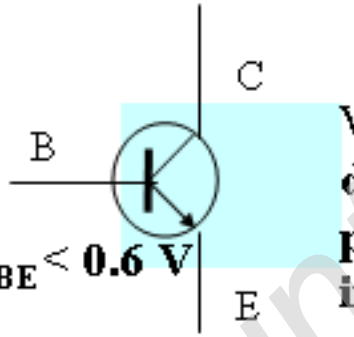


$V_{CE} = 0.2$ V

$V_{BE} = 0.6$ V

Interruttore chiuso

Transistor Interdetto

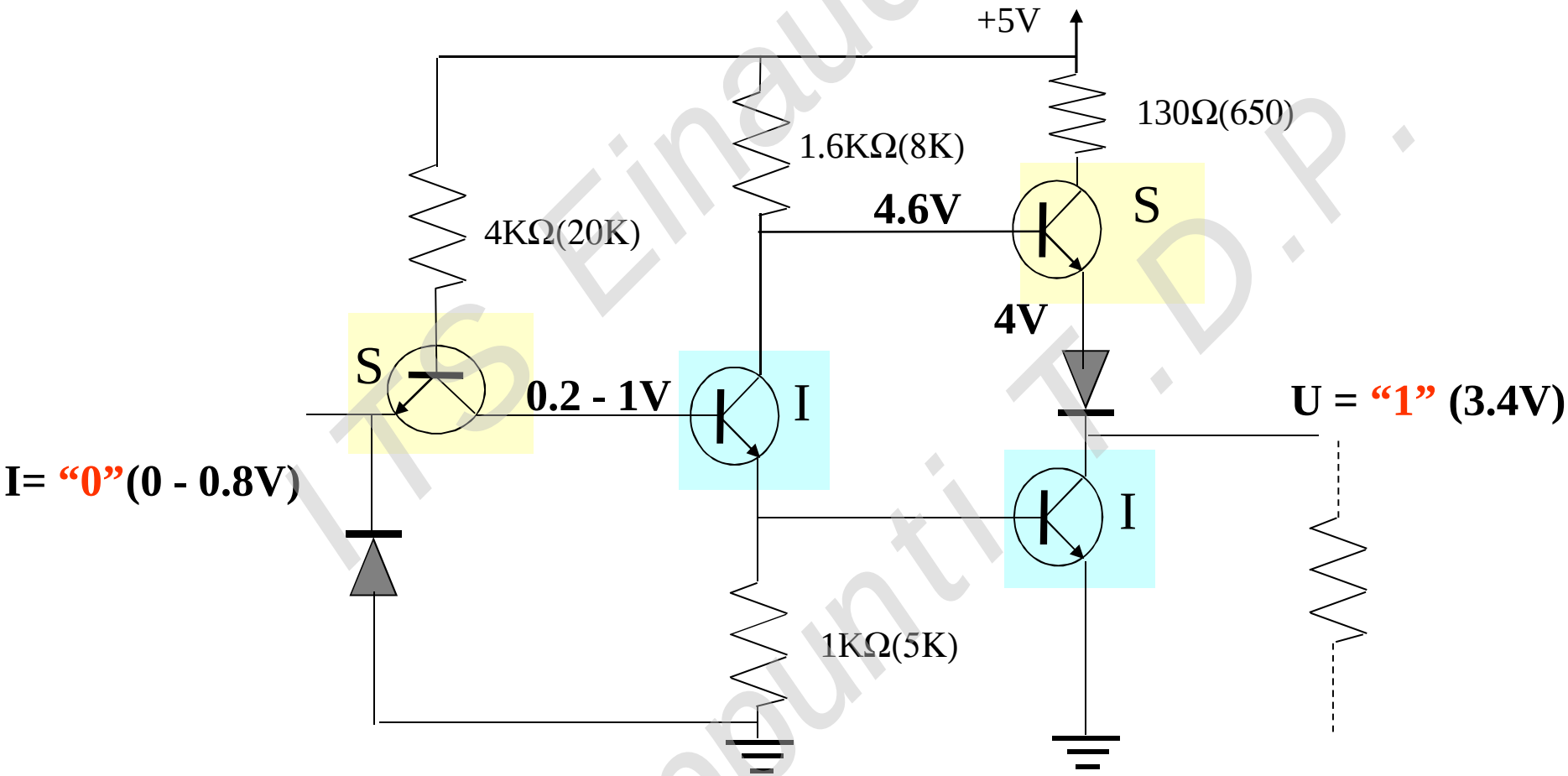


V_{CE} = dipende dal potenziale in C e E

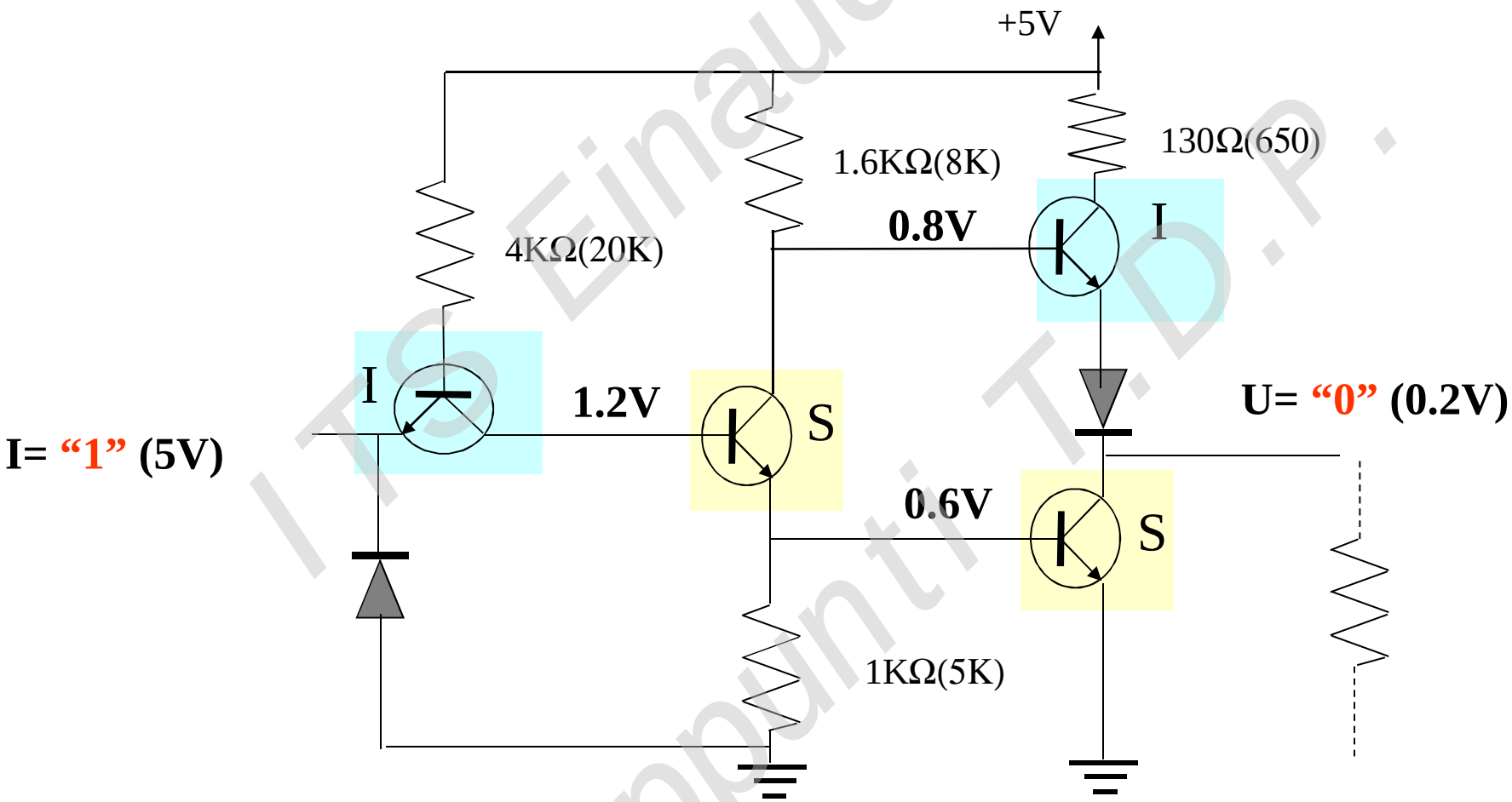
$V_{BE} < 0.6$ V

Interruttore aperto

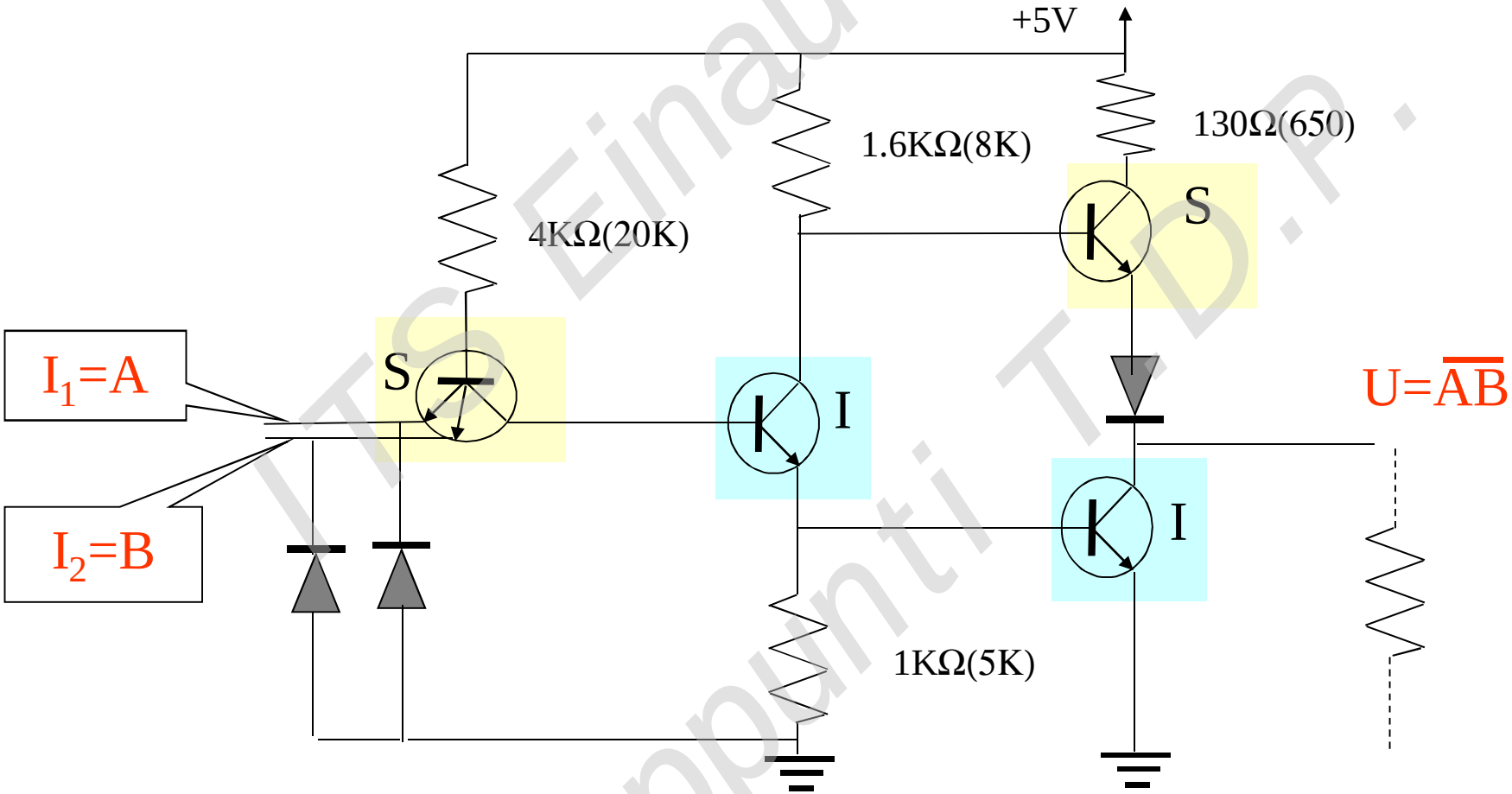
Porta NOT TTL totem-pole



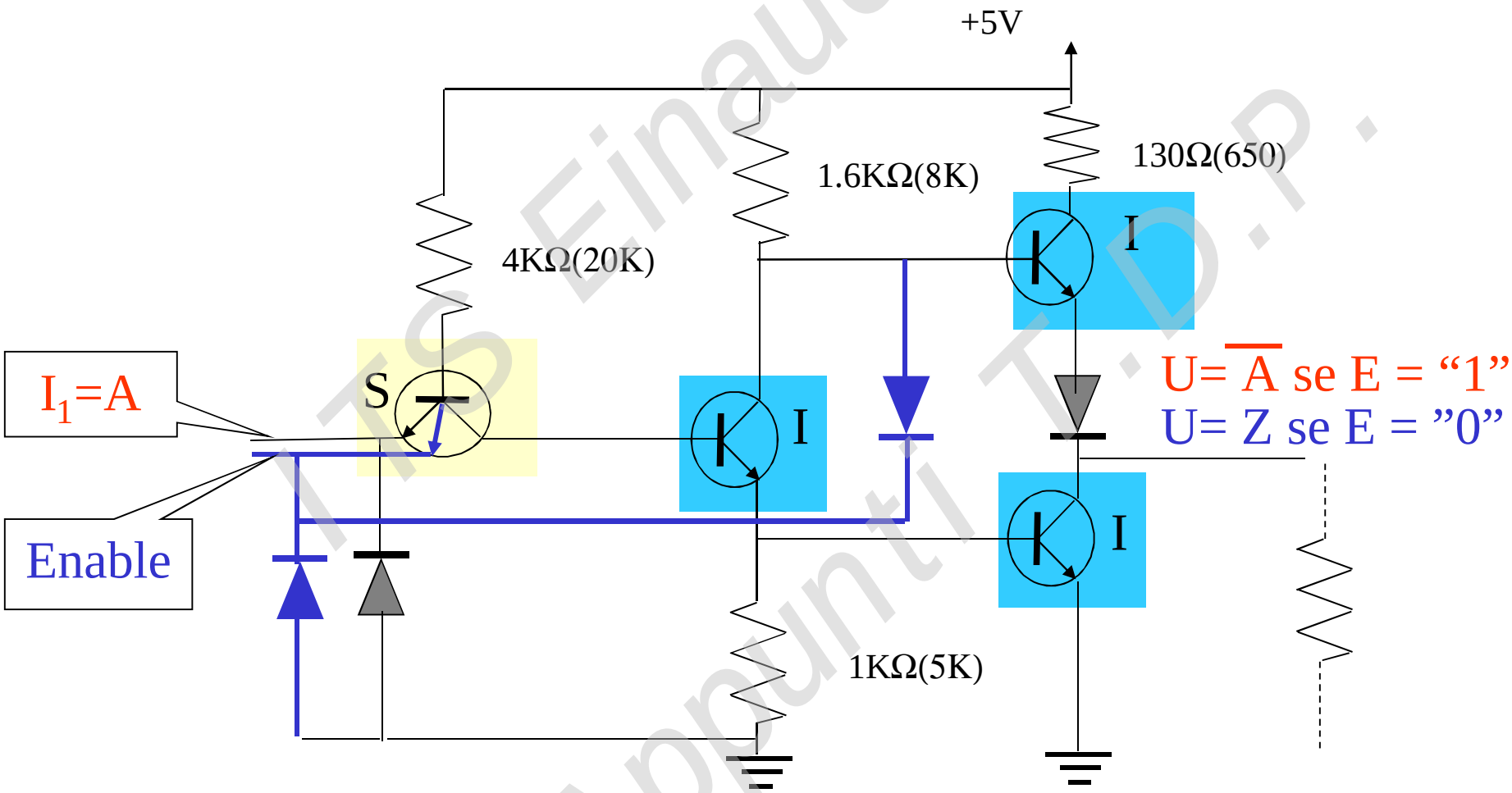
Porta NOT TTL totem-pole



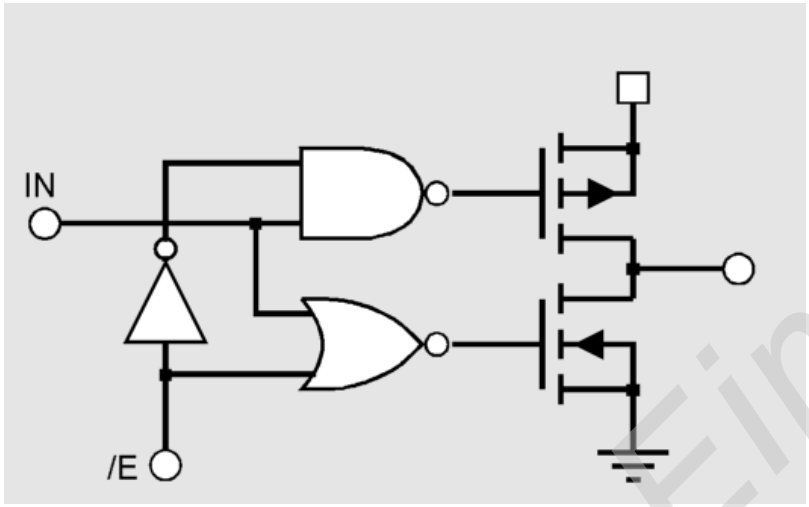
Porta NAND TTL totem-pole

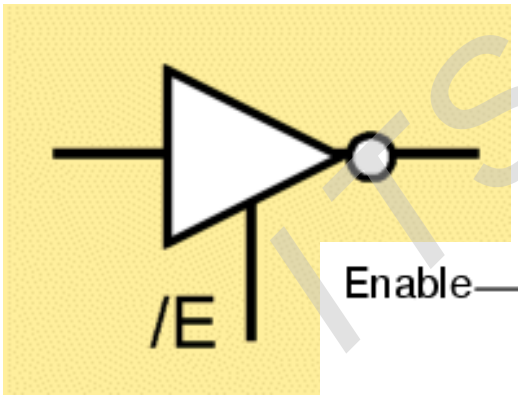


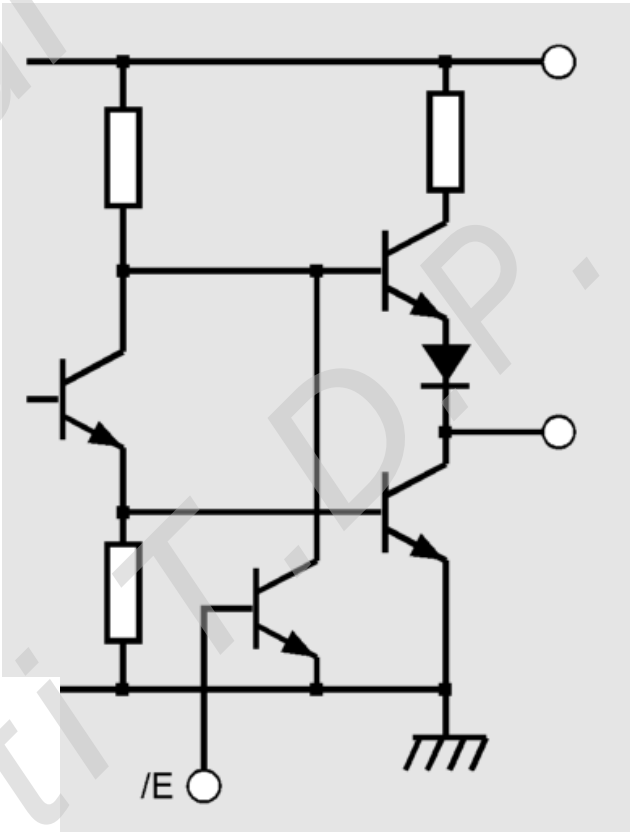
Porta NOT TTL totem-pole con uscita Three state

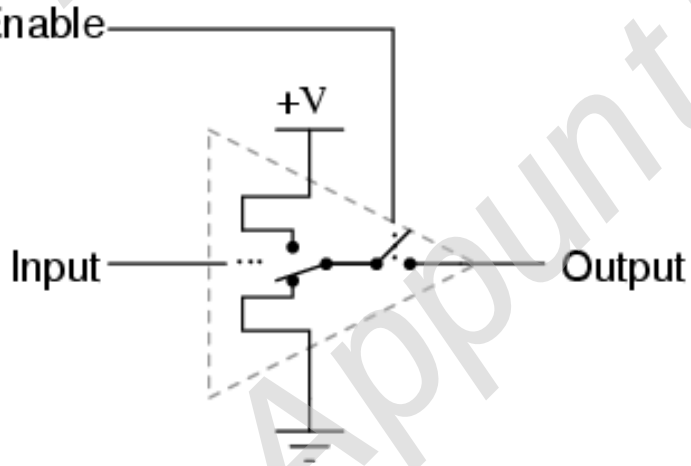


PORTE LOGICHE - logiche “tri-state”

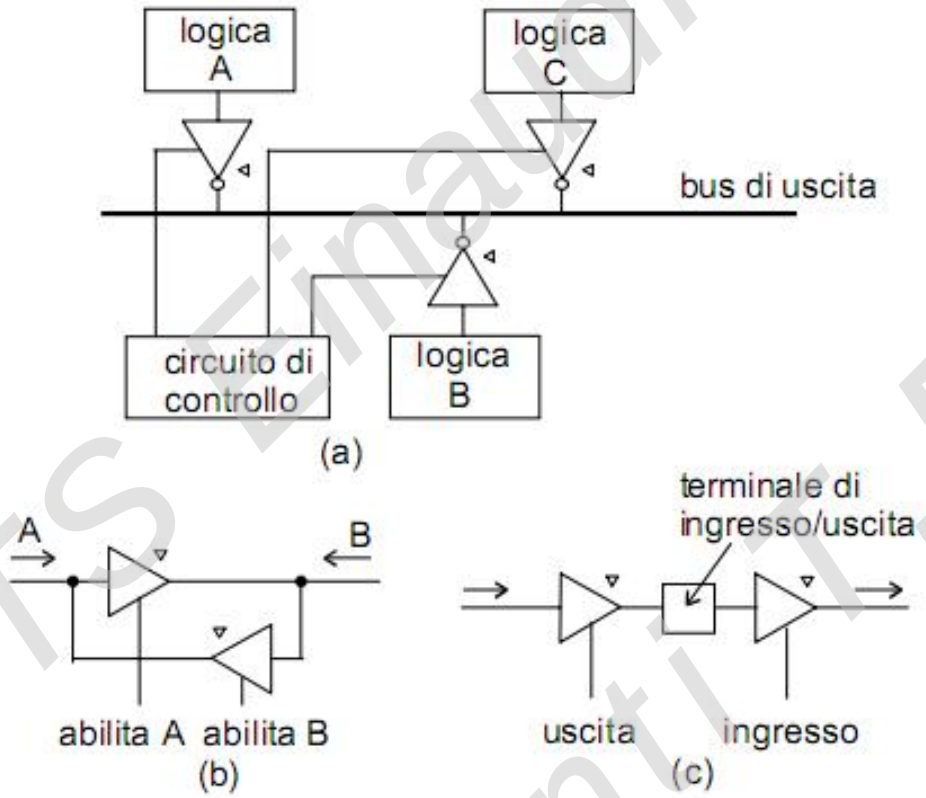








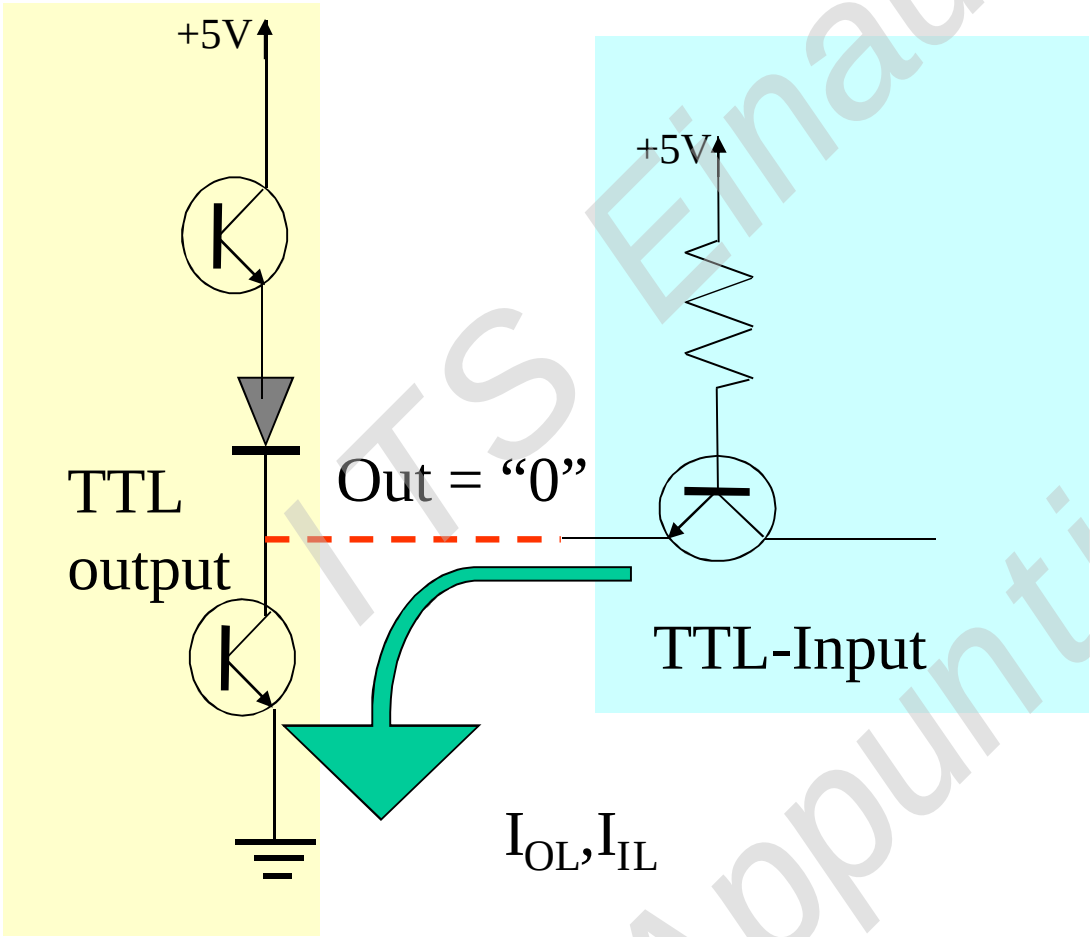
Applicazioni delle porte a tre stati



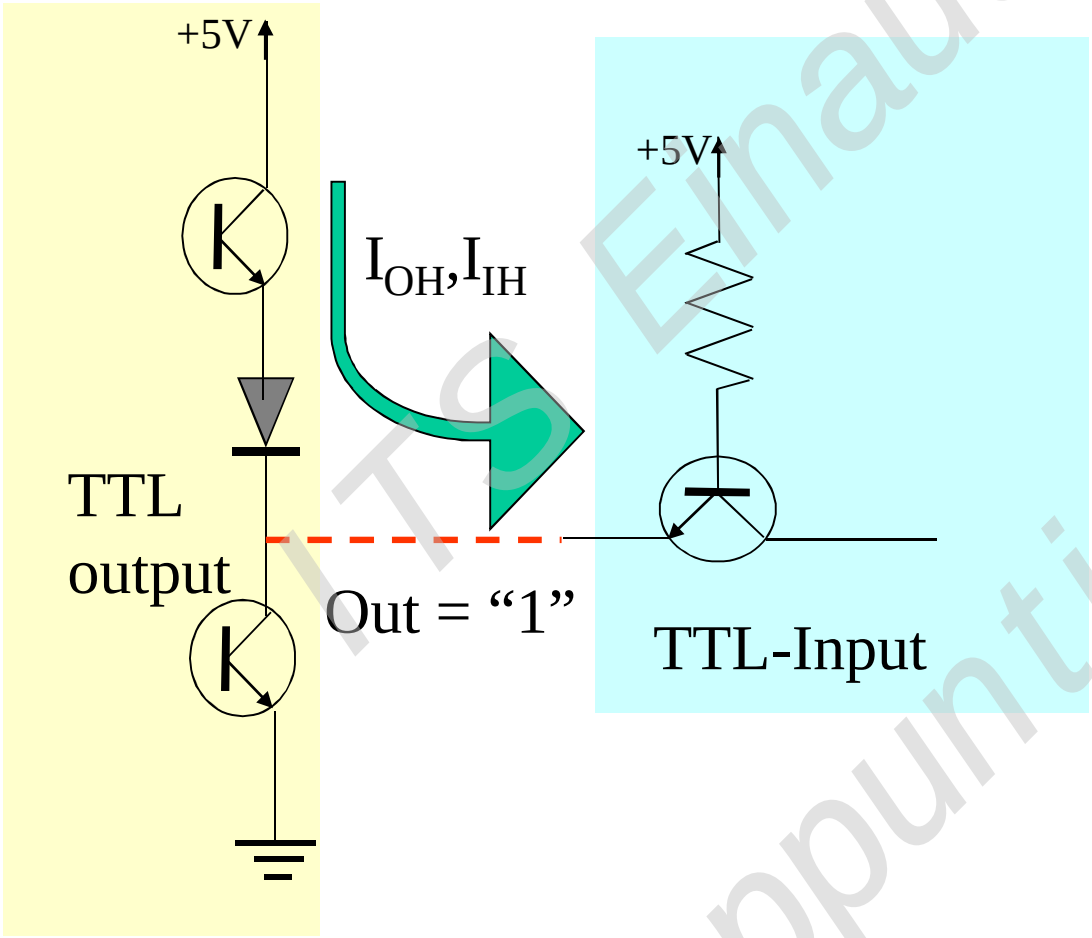
a) Connessioni multiple a un singolo bus di uscita

b) Buffer bidirezionale

c) Terminale ingresso-uscita

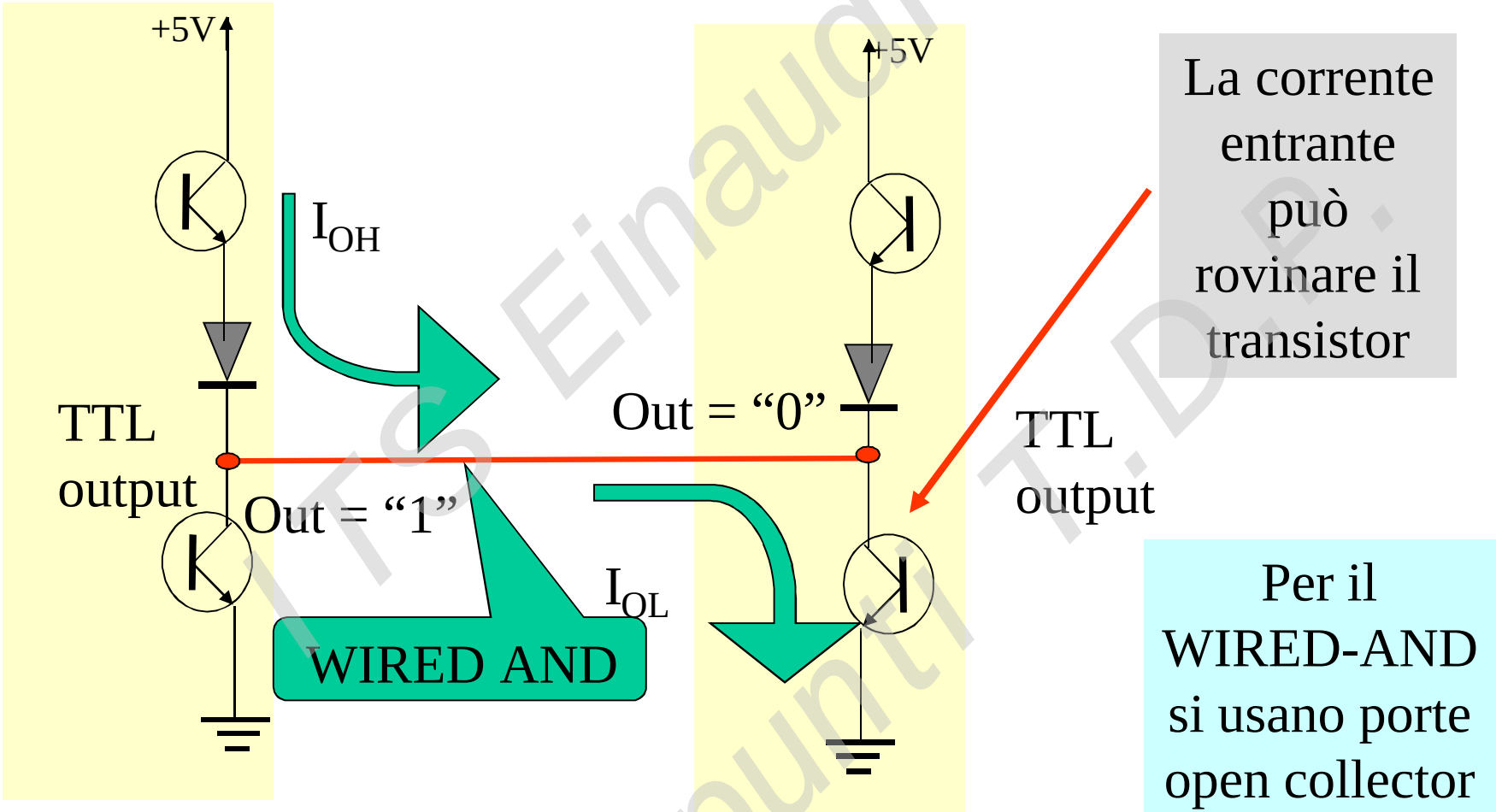


Il rapporto I_{OL}/I_{IL} definisce il **“fan –out”** ovvero il massimo numero di porte pilotabili



Anche il rapporto I_{OH}/I_{IH} è coerente con il fan-out

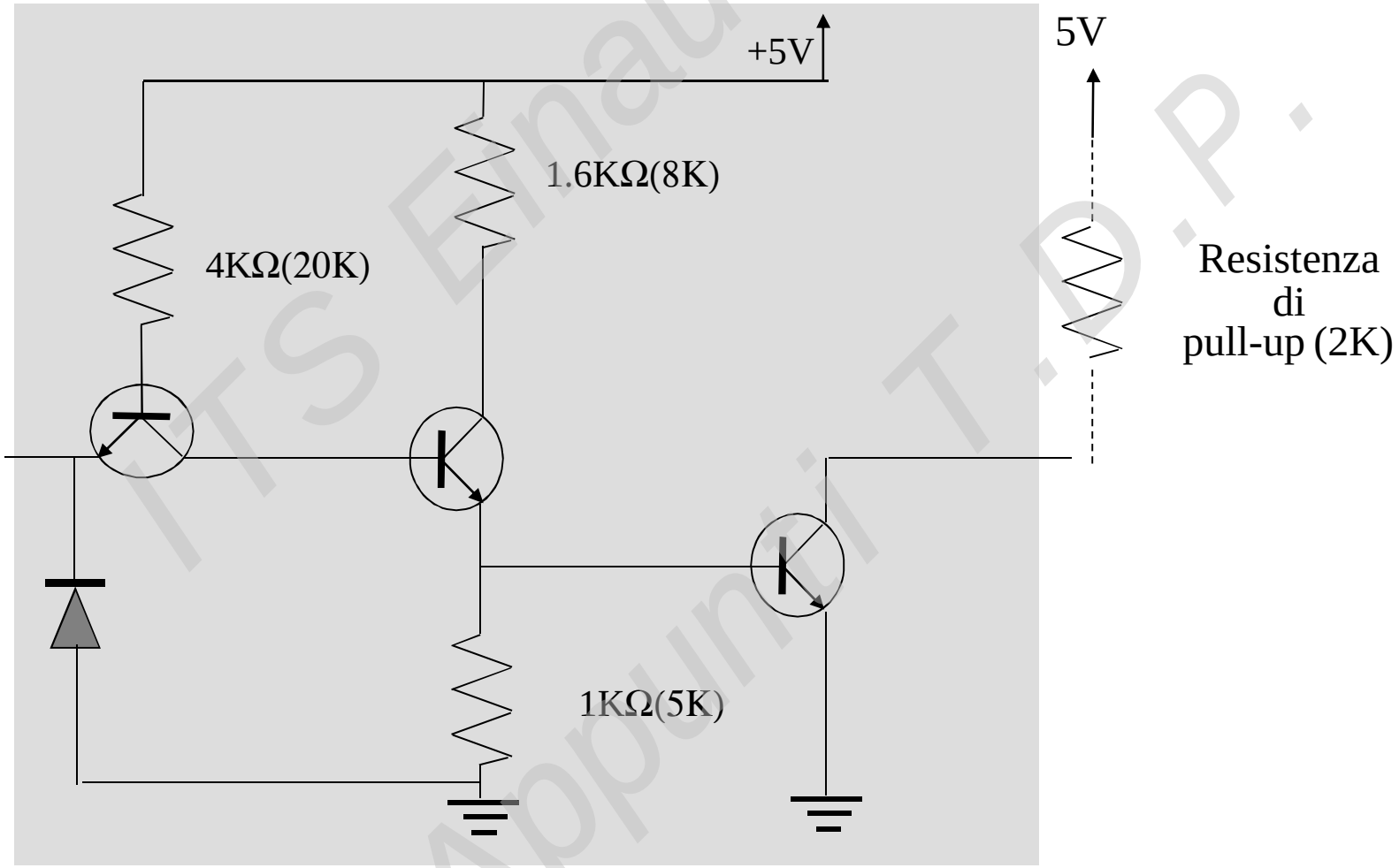
Logiche WIRED AND



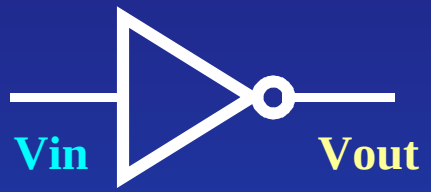
La corrente entrante può rovinare il transistor

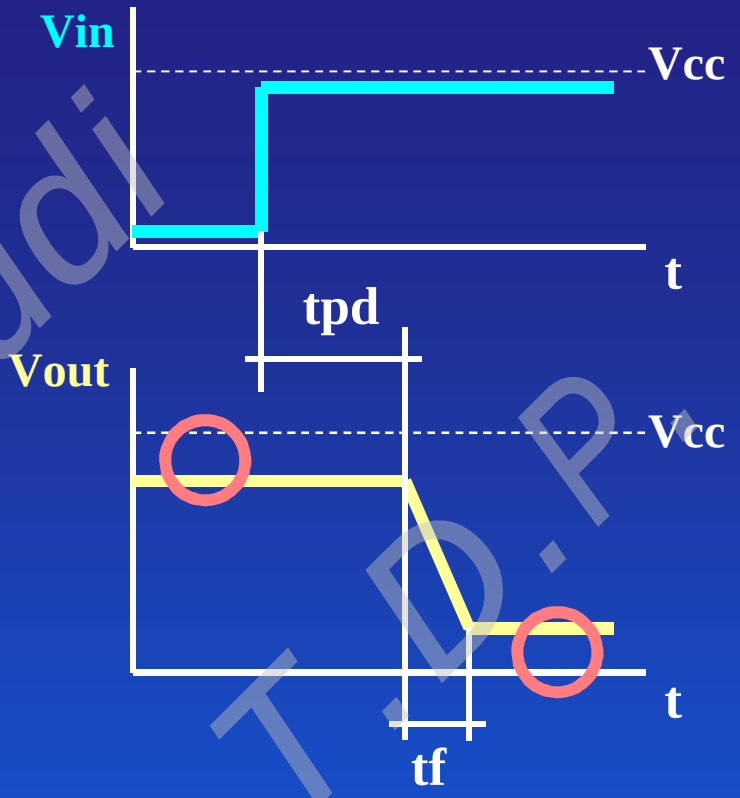
Per il WIRED-AND si usano porte open collector

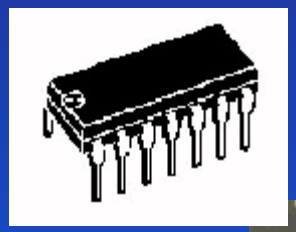
Porta NOT TTL open collector

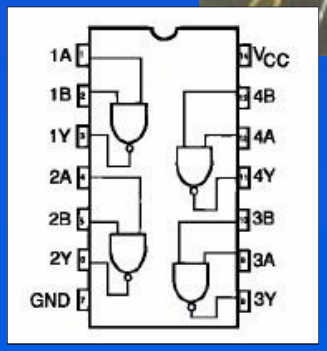


PORTE LOGICHE - le anomalie







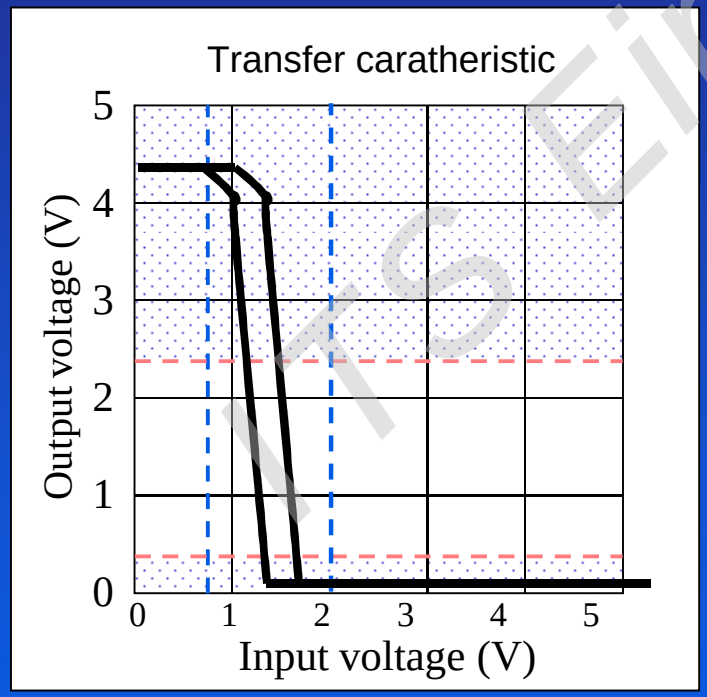


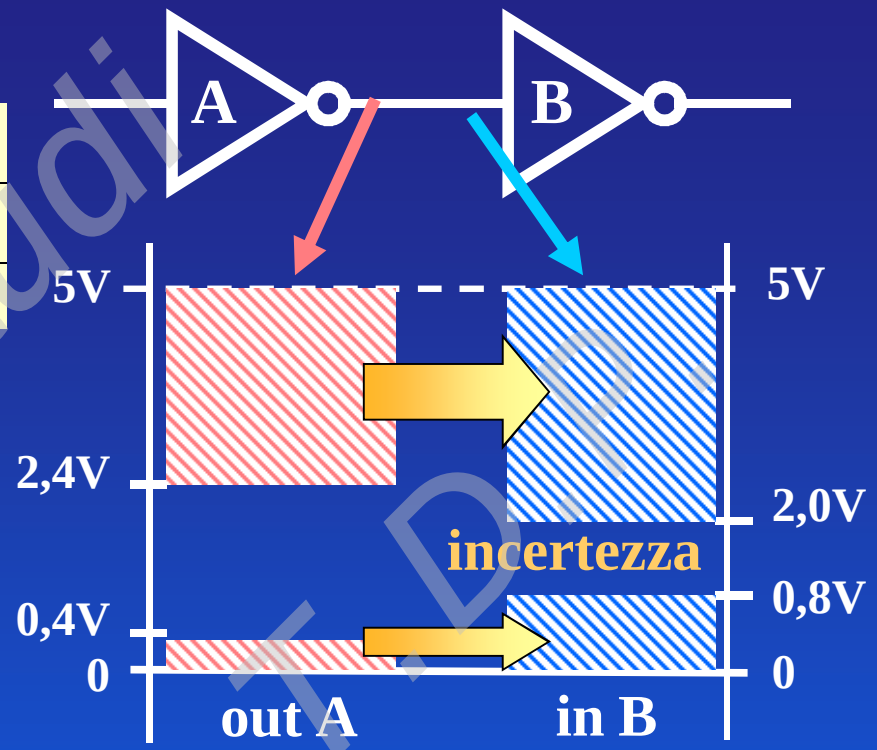
molteplici anomalie:

- livelli logici NON ideali
- ritardo di commutazione
- segnali trapezoidali
- derive termiche, ecc

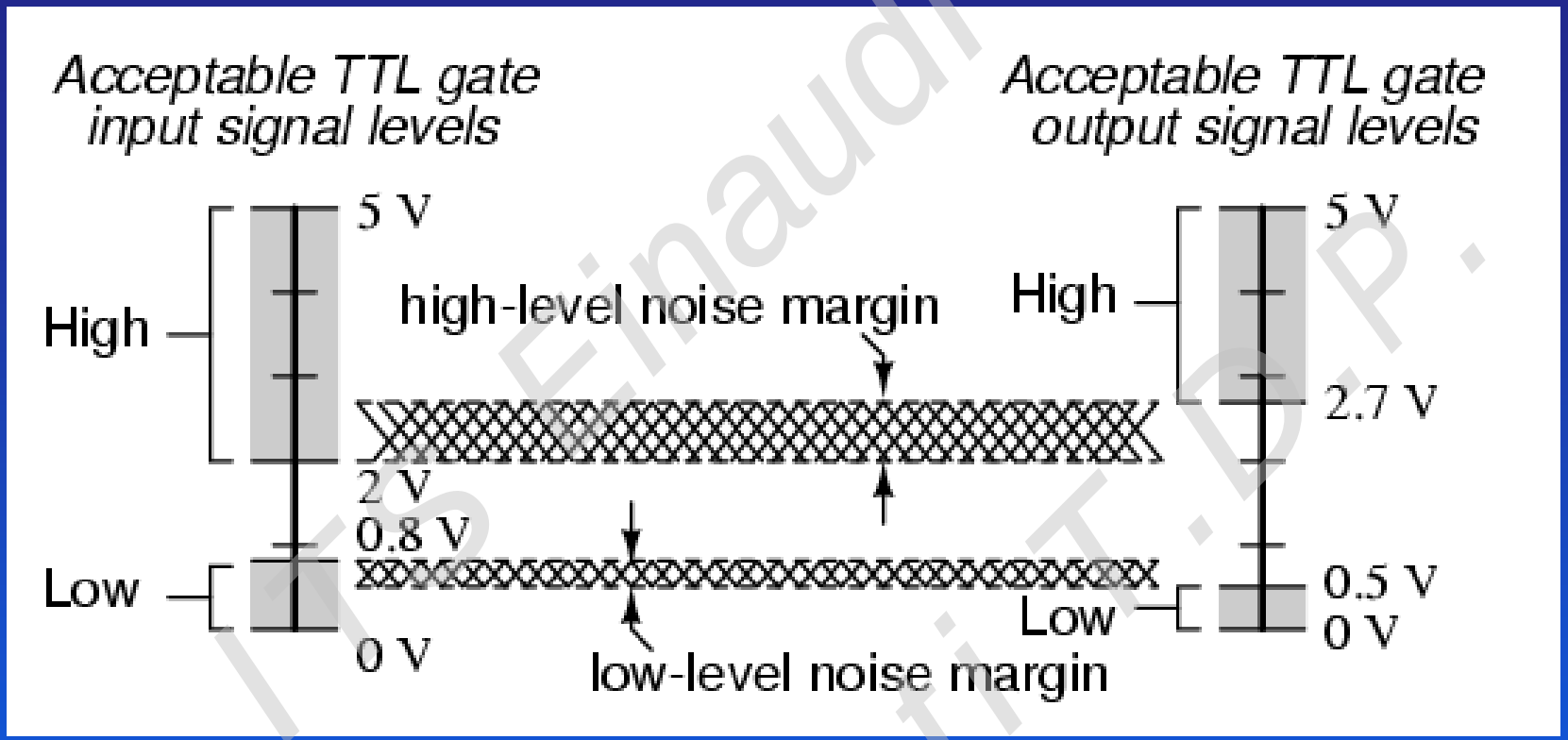
PORTE LOGICHE - i livelli logici

famiglia	V_{IH}	V_{IL}	V_{OH}	V_{OL}
TTL	**2,0 V**	**0,8 V**	**2,4 V**	**0,4 V**
LS-TTL	2,0 V	0,8 V	2,7 V	0,5 V





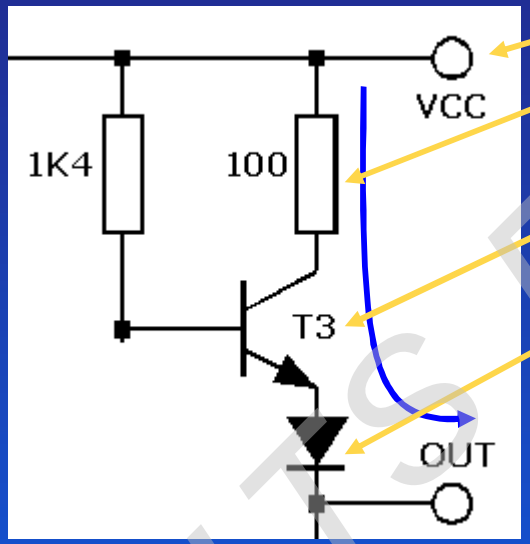
param.	conditions	min	typ	max	units
V_{OH}	Vcc=4.5V, 70°C, Io= -0.4mA, Vin=0.8V	2.4	3.3		V
V_{OL}	Vcc=4.5V, 70°C, Io=16mA, Vin=2V		0.22	0.4	V

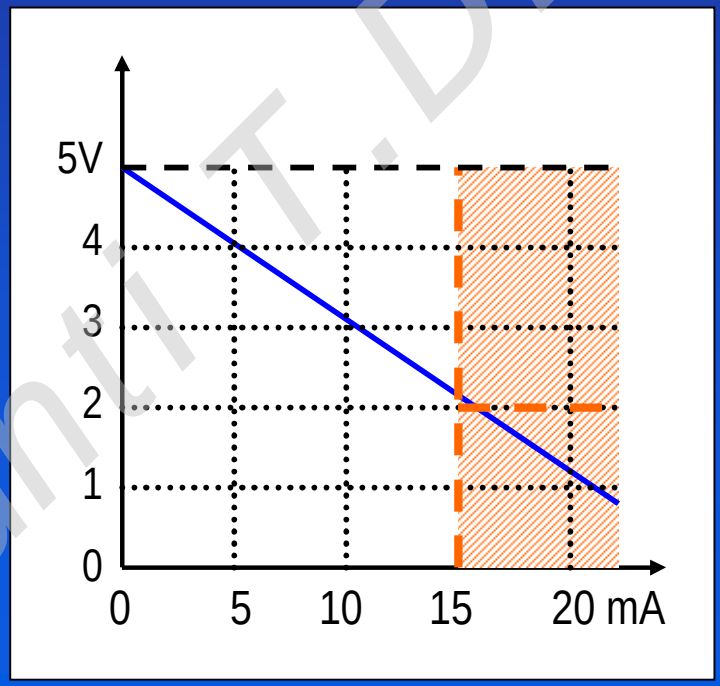


PORTE LOGICHE

- la tensione d'uscita è funzione della corrente

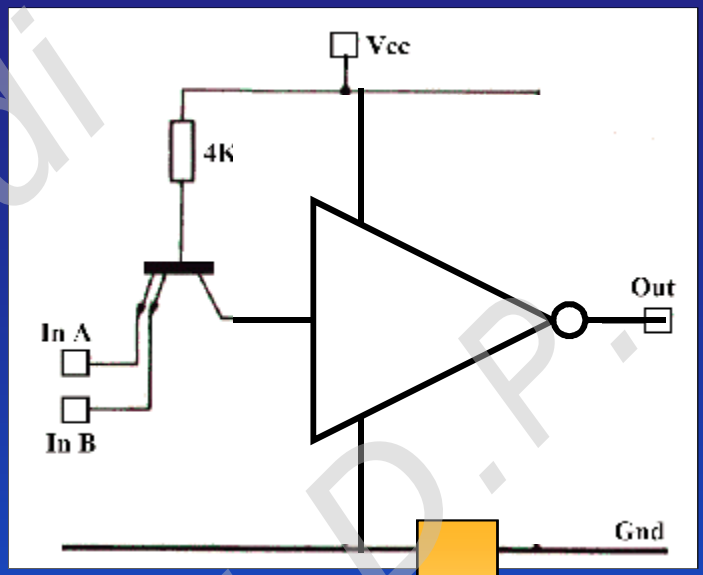
$$Vo = Vcc - R \cdot Io - V_{CE(SAT)} - 0.7$$





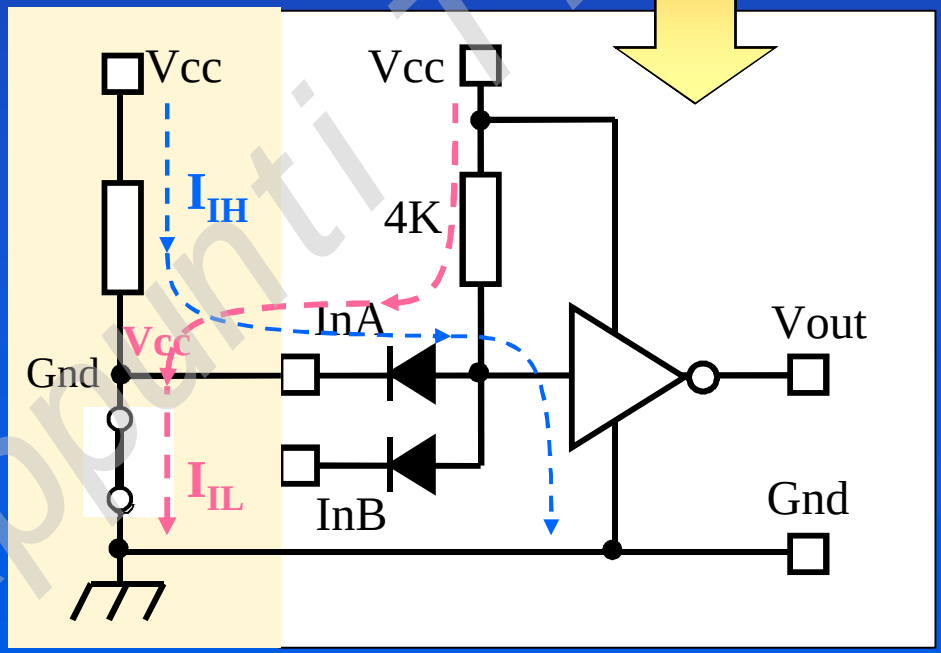
PORTE LOGICHE - le correnti d'ingresso

schema interno
di una porta TTL
(Nand a 2 ingressi)



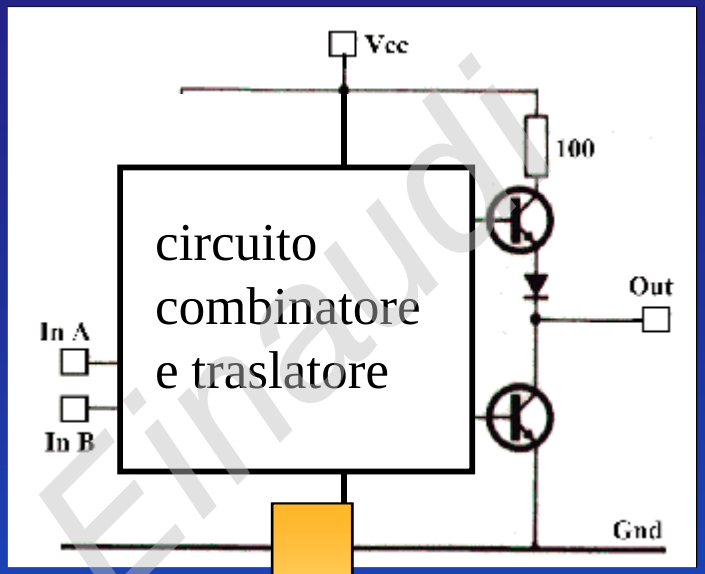
circuito equivalente d'ingresso

param	min	max	units
I_{IH}		40	µA
R_{IN}	100		Kohm
I_{IL}		-1.6	mA



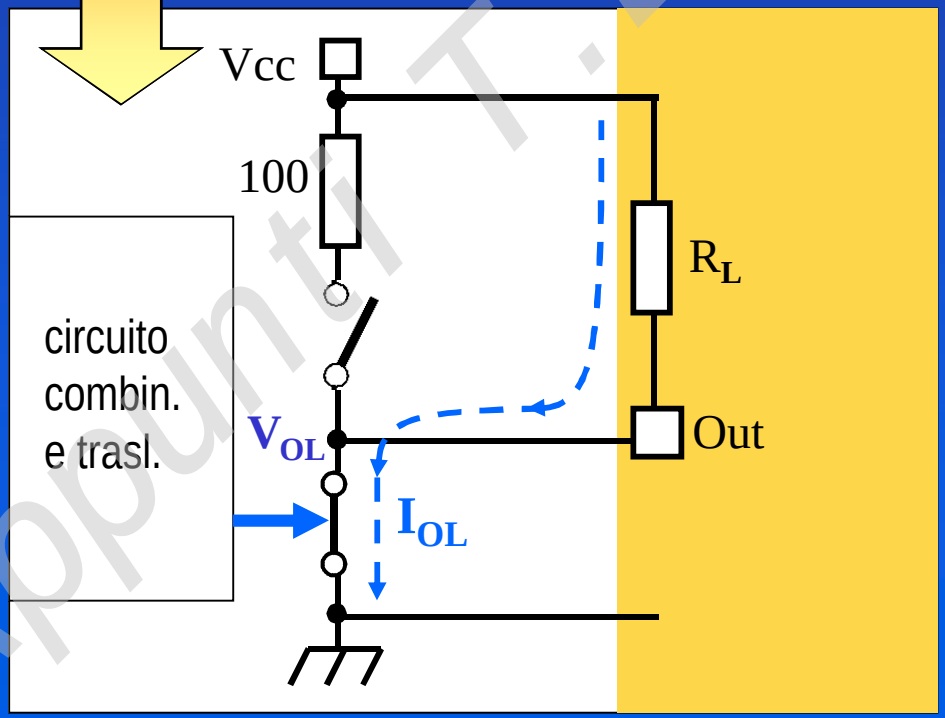
PORTE LOGICHE

- le correnti d'uscita



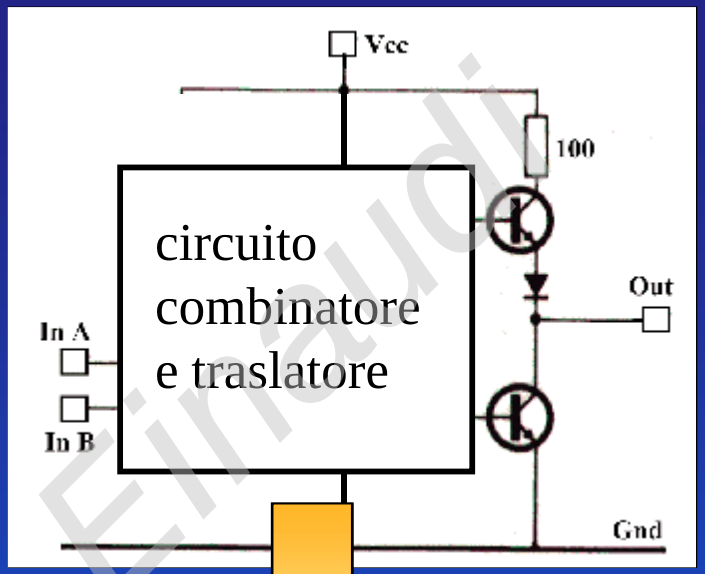
schema interno
di una porta TTL
(Nand a 2 ingressi)

param	min	max	units
I_{OH}		-13	mA
I_{OL}		25	mA
I_{OSC}		-55	mA



PORTE LOGICHE

- le correnti d'uscita



schema interno
di una porta TTL
(Nand a 2 ingressi)

param	min	max	units
I_{OH}		-13	mA
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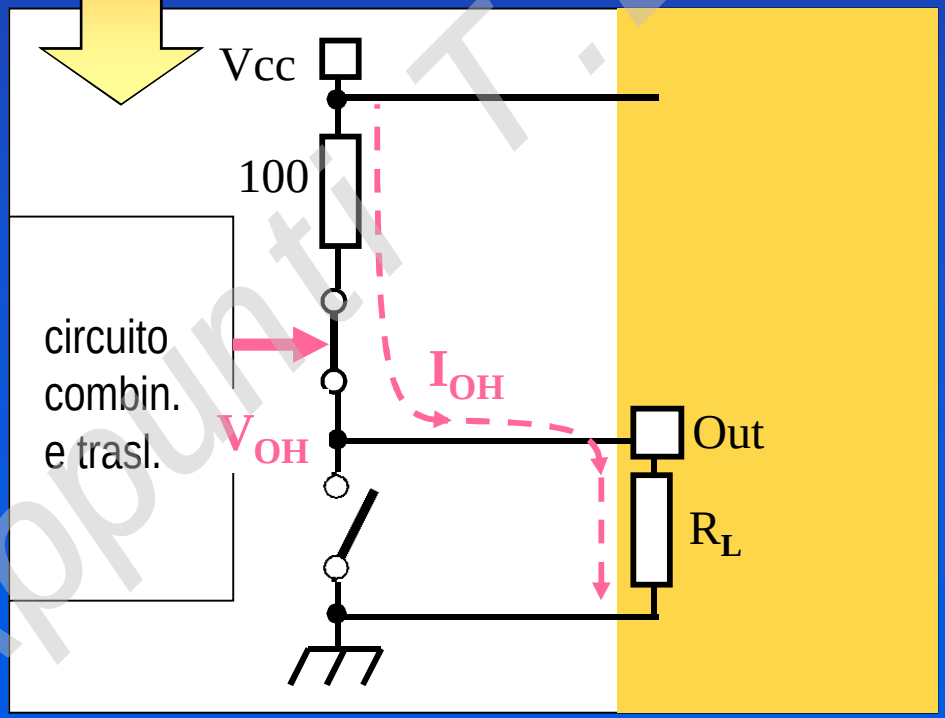
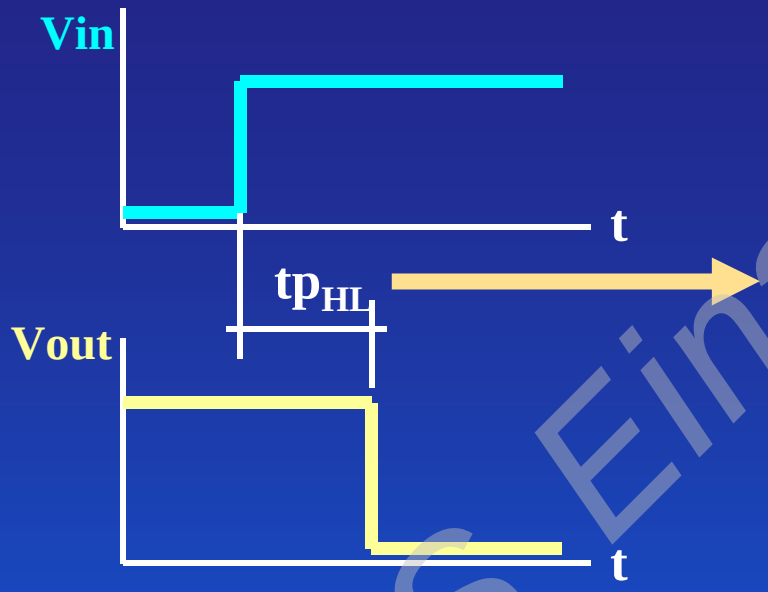
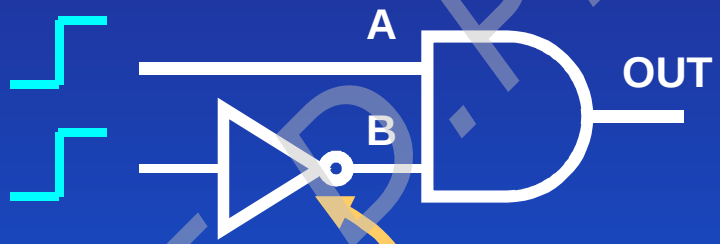


PORTE LOGICHE - il tempo di propagazione

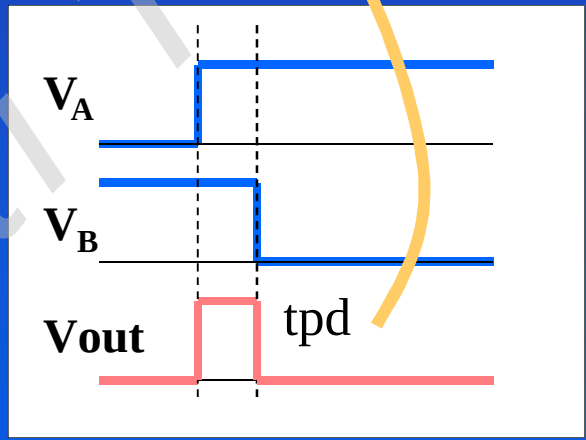


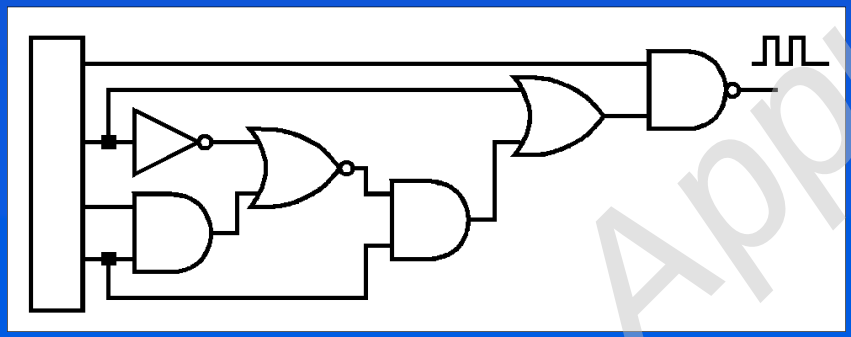
tpd = Propagation Delay Time
(tempo di propagazione)

è il ritardo con cui l'uscita della logica commuta rispetto all'istante in cui commuta l'ingresso



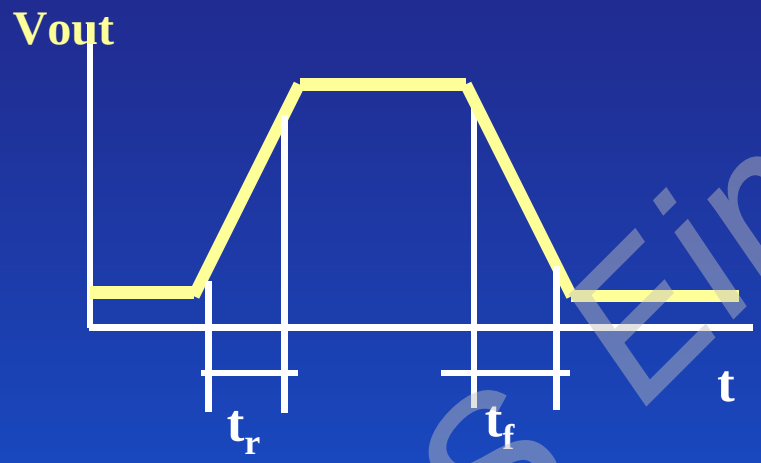
param.	typ	max	units
tp_{LH}	8	12	nsec
tp_{HL}	12	18	nsec

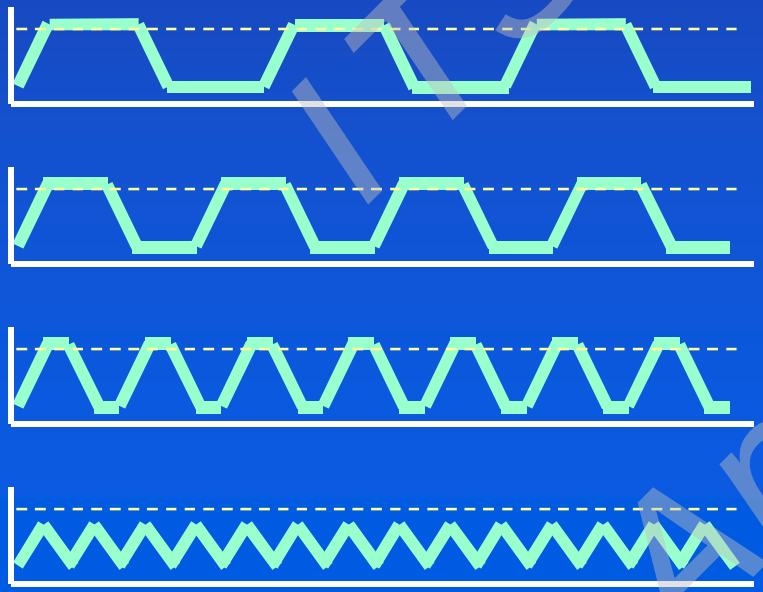


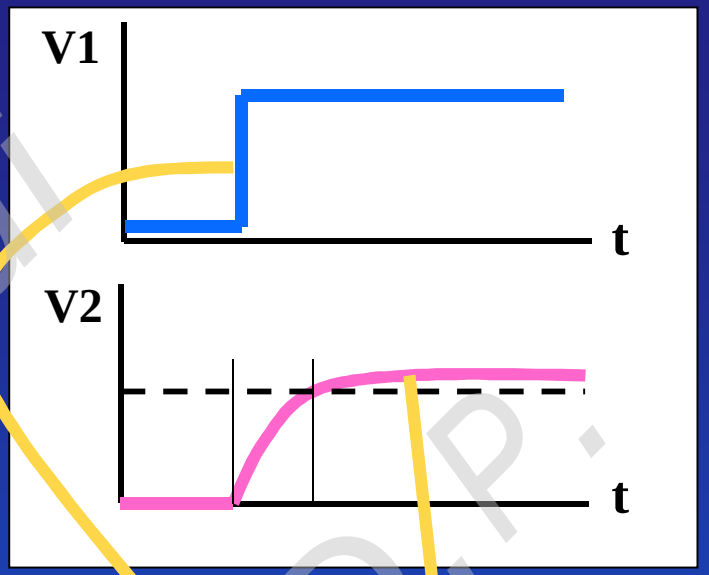


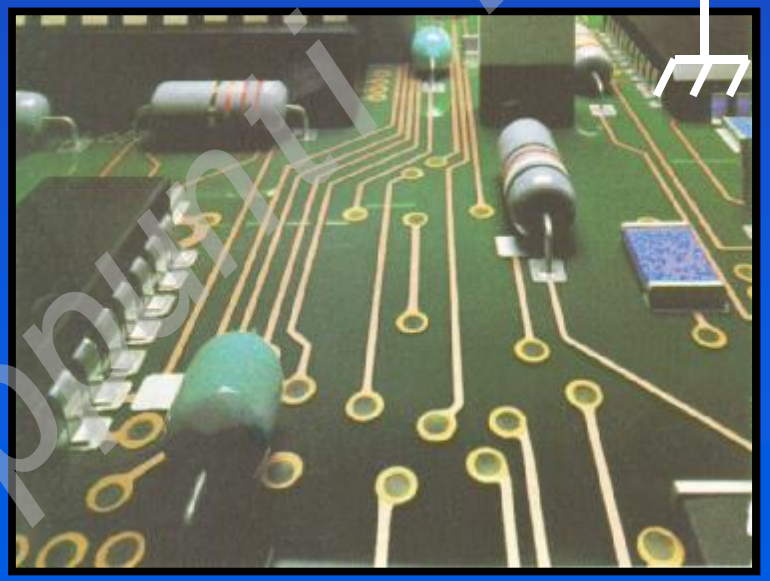
PORTE LOGICHE

- i tempi di salita e discesa



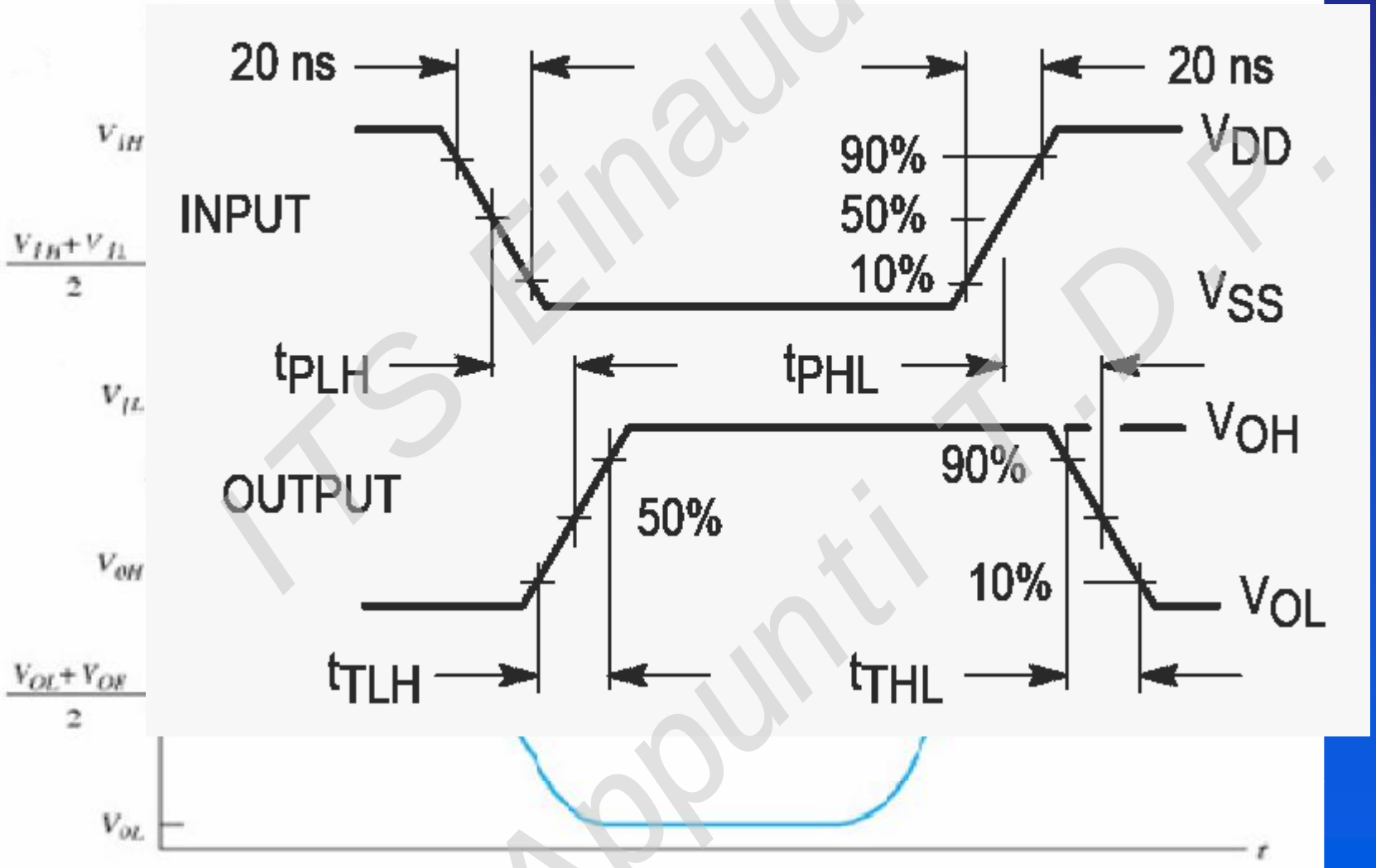






PORTE LOGICHE

- i tempi : definizioni



PORTE LOGICHE
- i tempi : definizioni

t_f tempo di discesa del segnale di uscita misurato tra il 90% e il 10 % della tensione di uscita massima V_{OH}

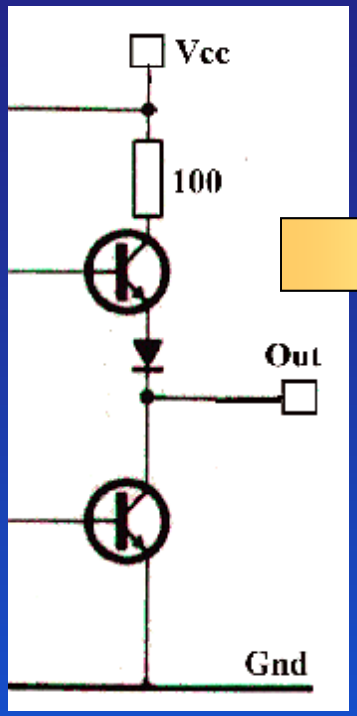
t_r tempo di salita del segnale di uscita. E' il tempo necessario affinché l'uscita passi dal 10% al 90 % del valore massimo V_{OH}

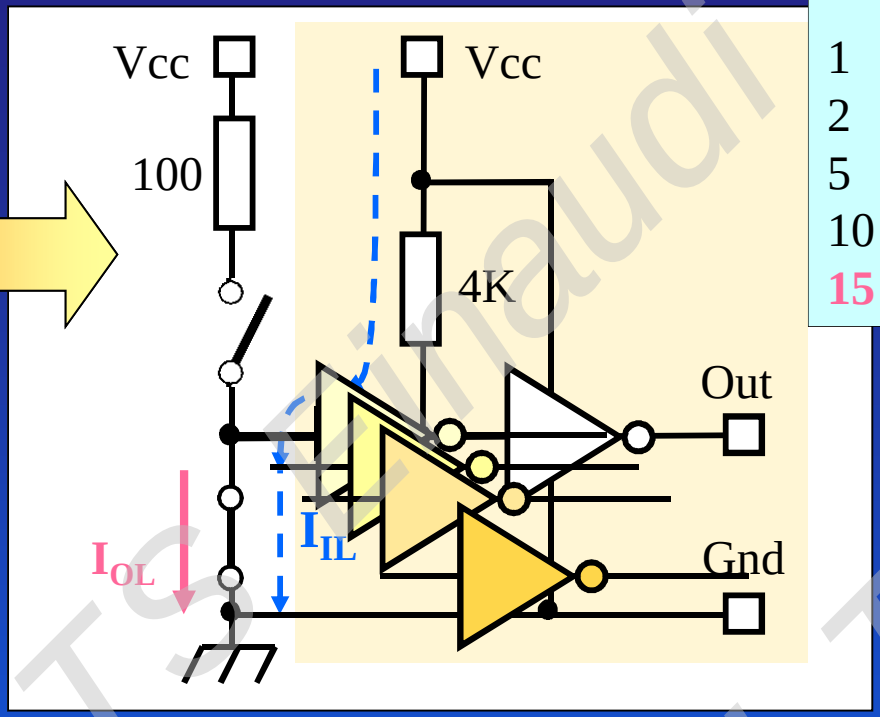
t_{pHL} tempo di ritardo di propagazione dal livello alto al livello basso. E' misurato come l'intervallo di tempo tra il 50% di V_{IHM} e il 50 % di V_{OHM}

t_{pLH} tempo di ritardo di propagazione dal livello basso al livello alto. E' misurato come l'intervallo di tempo tra il 50% di V_{IHM} e il 50 % di V_{OHM}

t_{pHL} e t_{pLH} sono, in genere, diversi tra loro e il costruttore fornisce il loro valor medio definito come tempo di ritardo di propagazione t_p

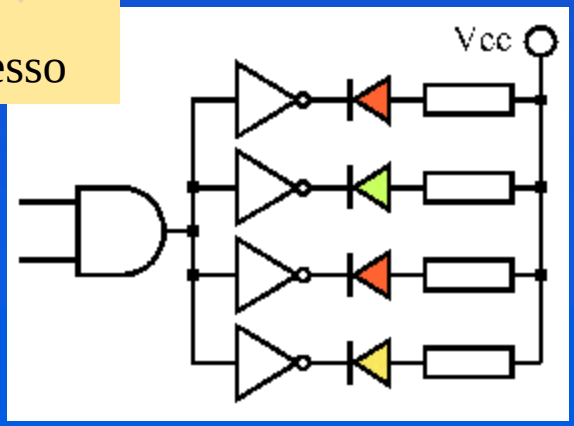
PORTE LOGICHE - il fan-out



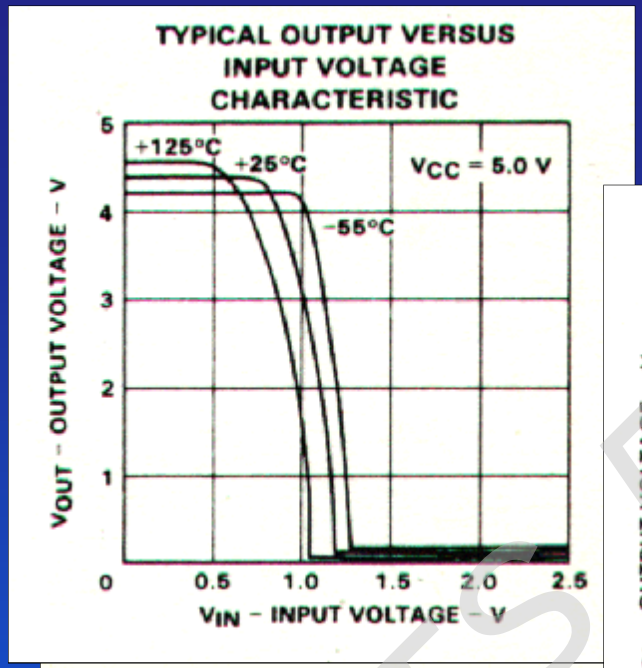


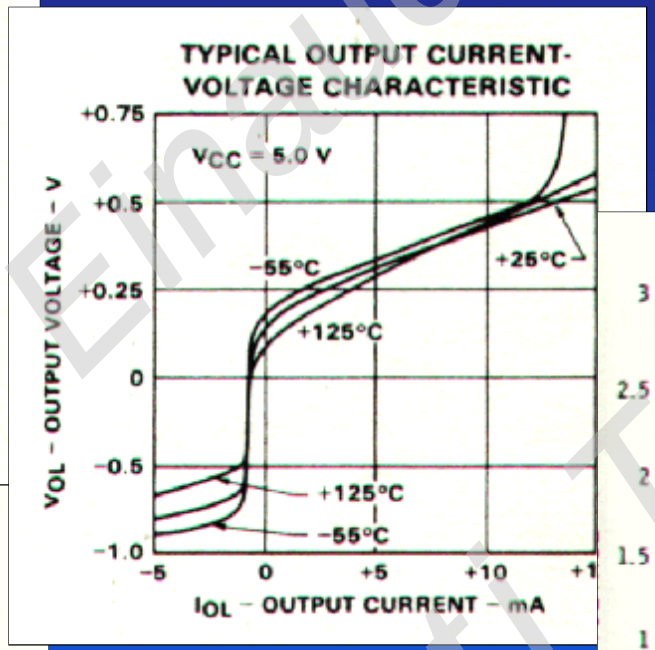
n° porte	R_{IN}	I_{IL}
1	4K	-1.6mA
2	2K	-3.2mA
5	0.8K	-8mA
10	0.4K	-16mA
15	**0.27K**	**-24mA**

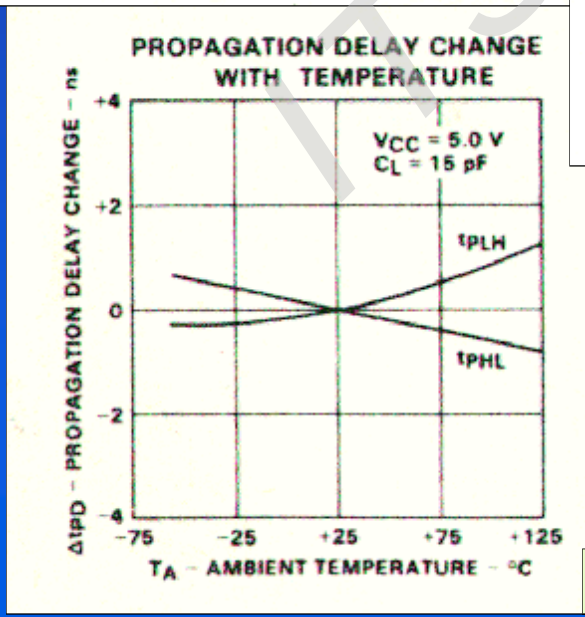
Il FAN-OUT rappresenta il massimo numero di porte logiche pilotabili da un'uscita, ed è equivalente al rapporto fra la massima corrente d'uscita e la massima corrente d'ingresso

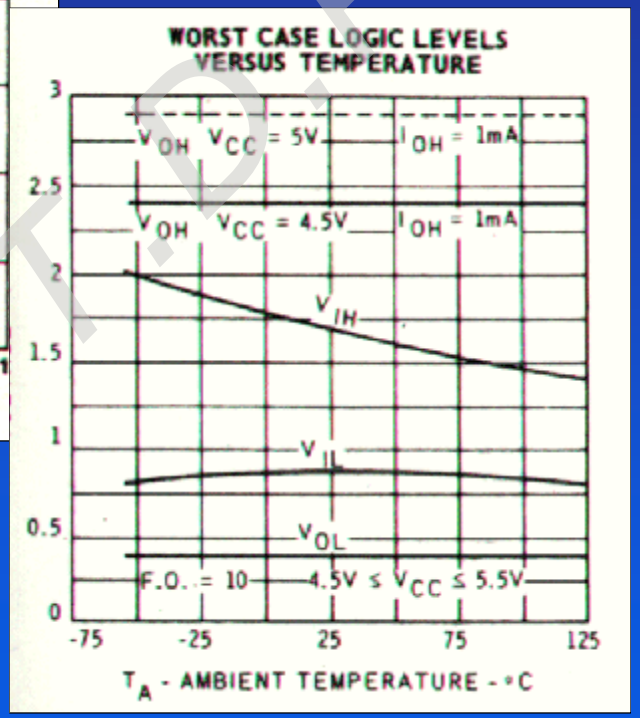


PORTE LOGICHE - le derive termiche

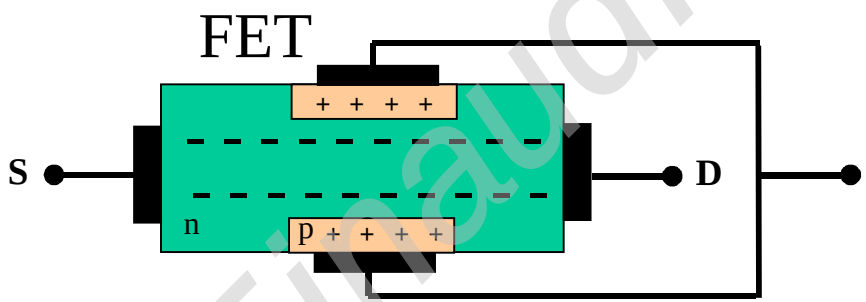


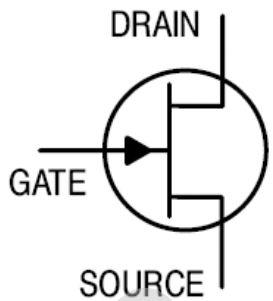


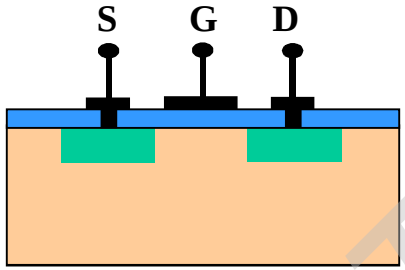




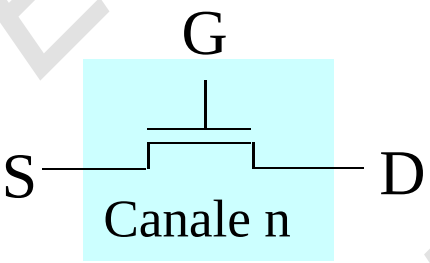
Porte CMOS

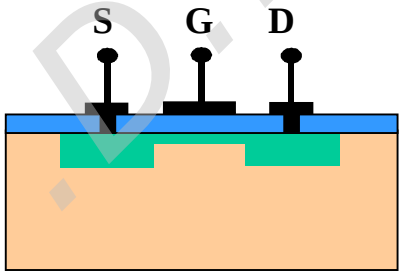






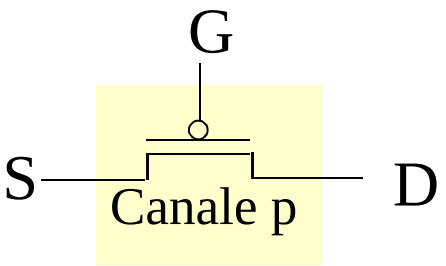
CMOS a enancement





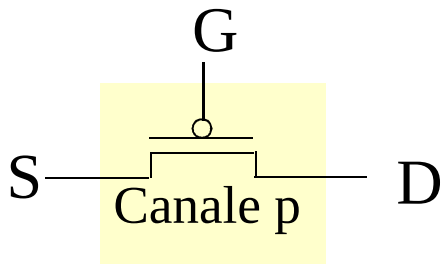
CMOS a depletion

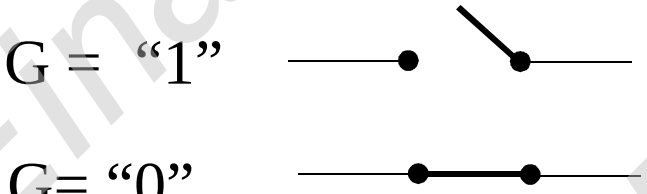
Il canale n con un “1” il transistor si comporta come un interruttore chiuso, mentre con uno “0” , come un interruttore aperto.

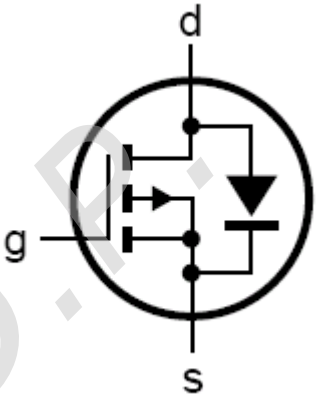


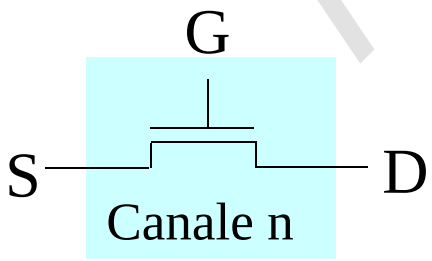
In modo simmetrico funziona il canale P

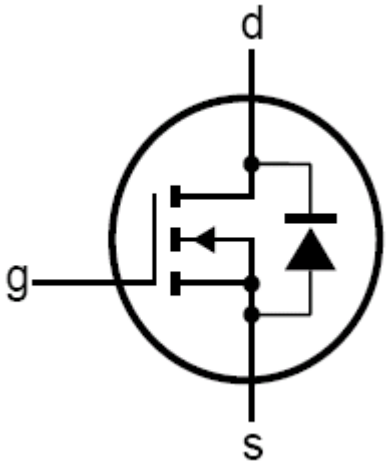
Porte CMOS



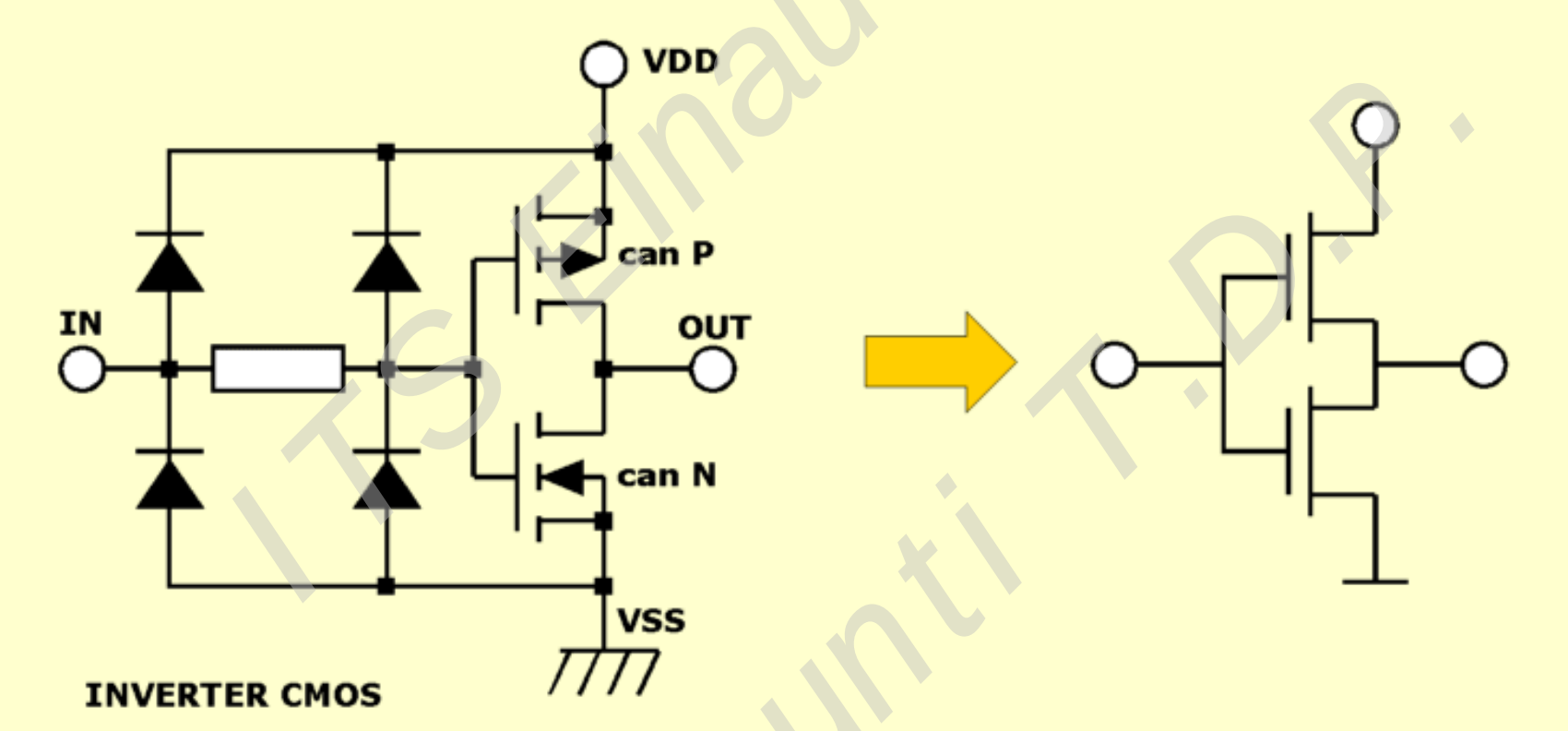


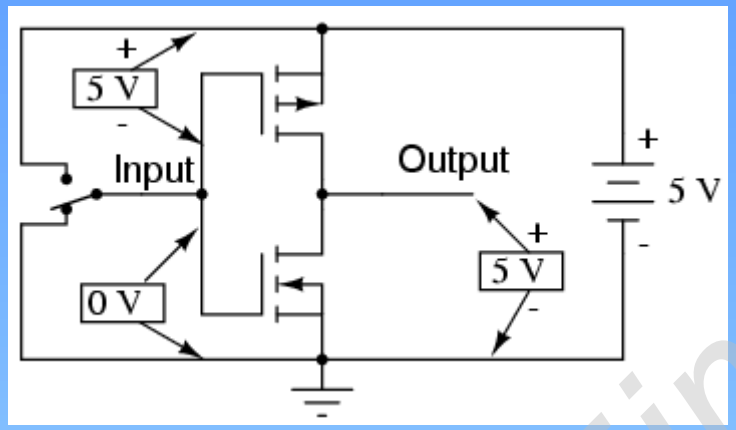


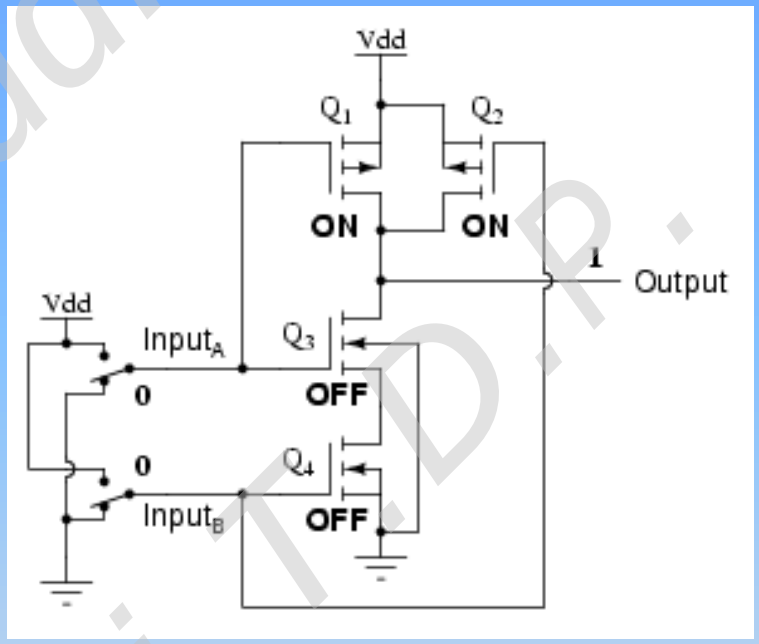


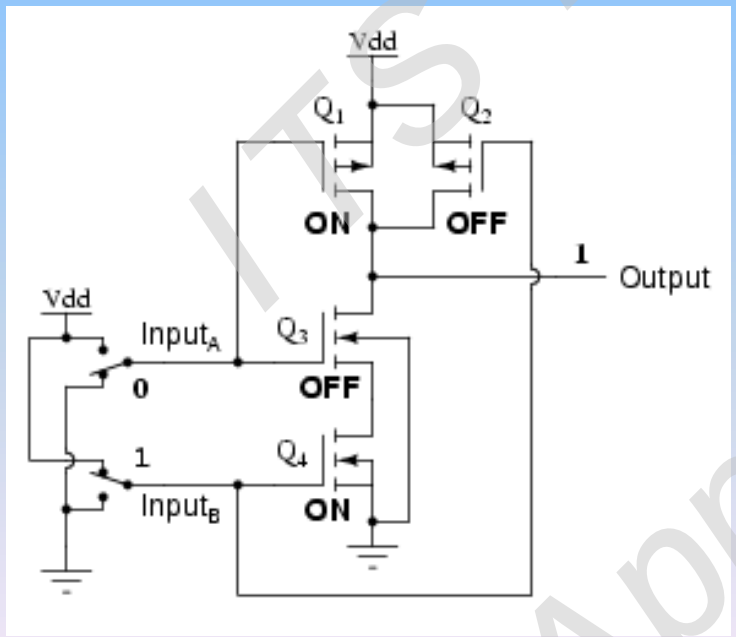


NOT CMOS

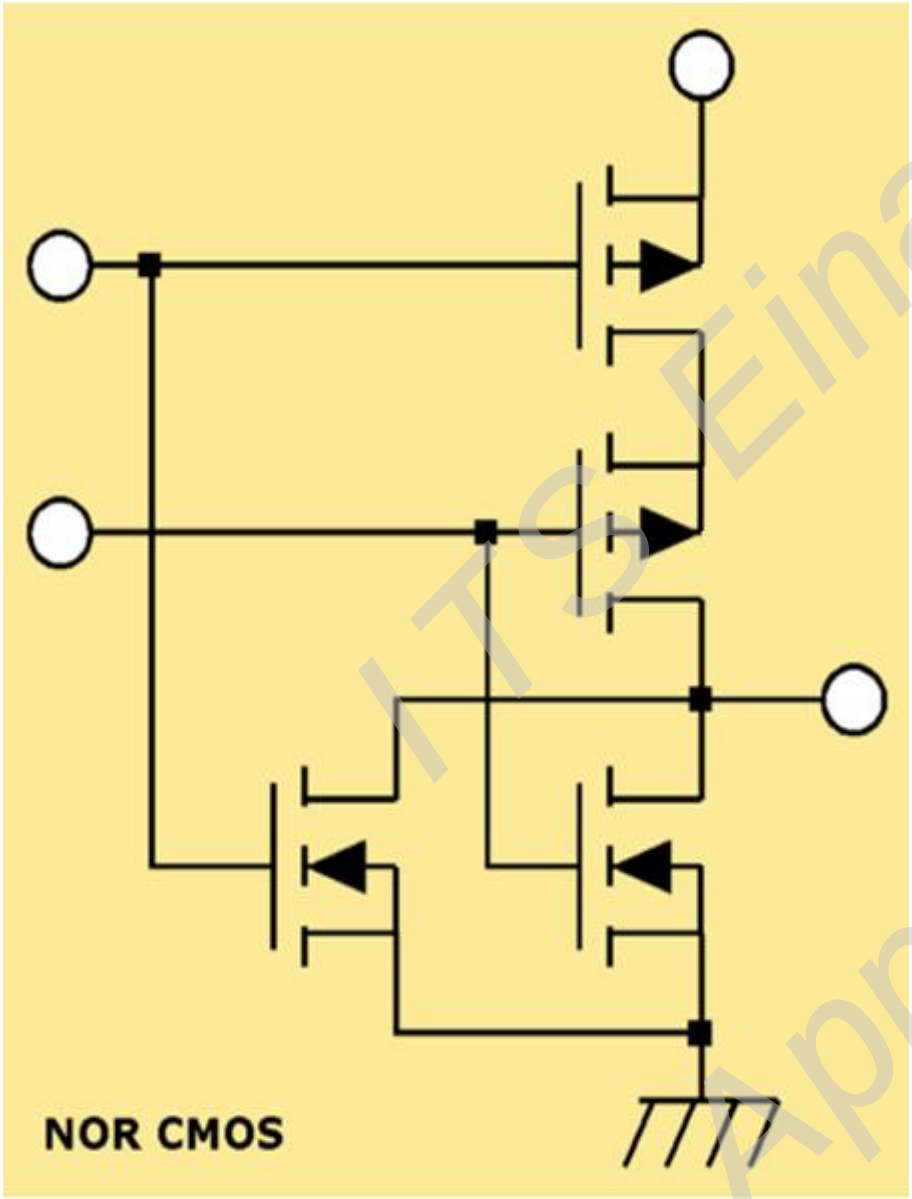


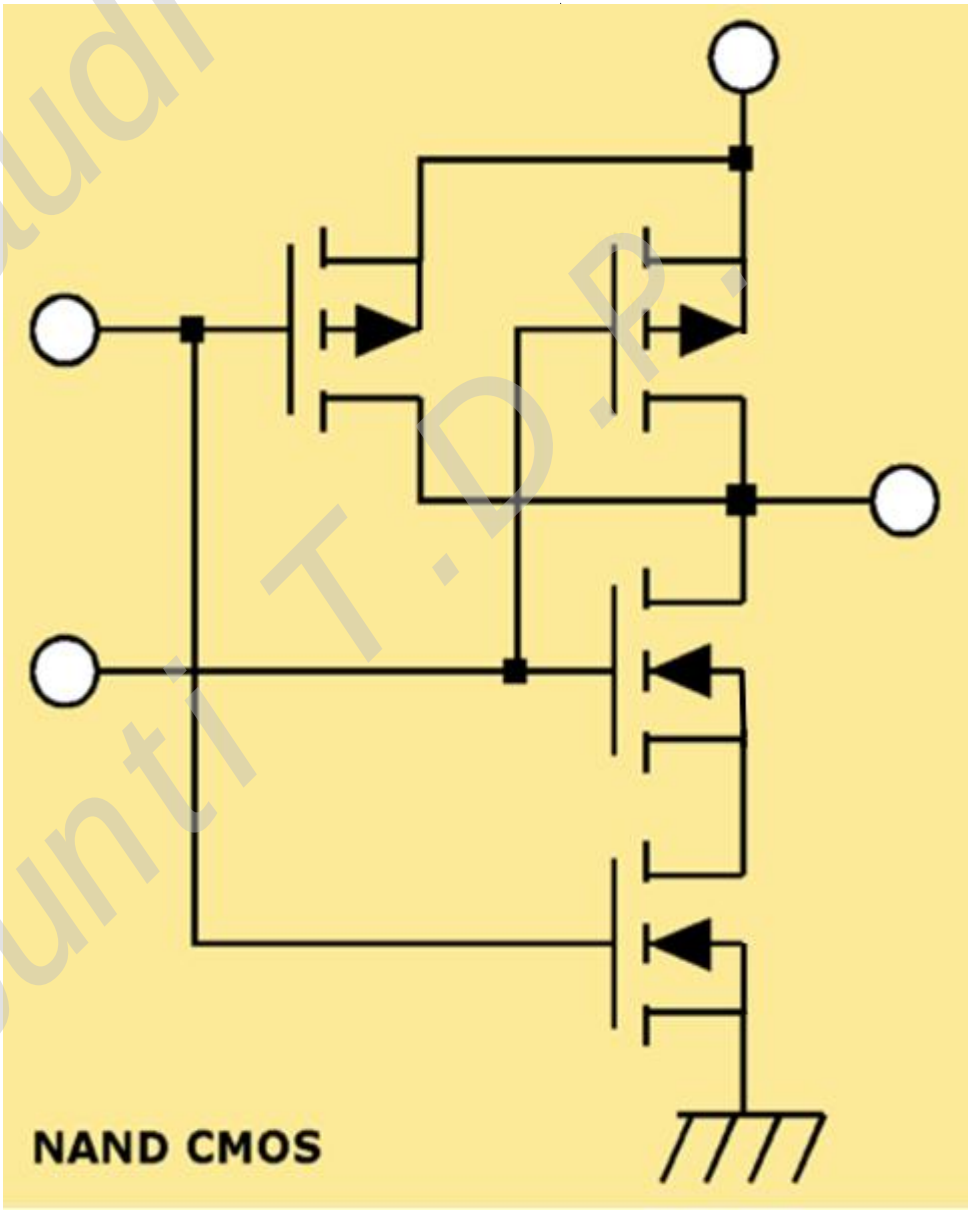




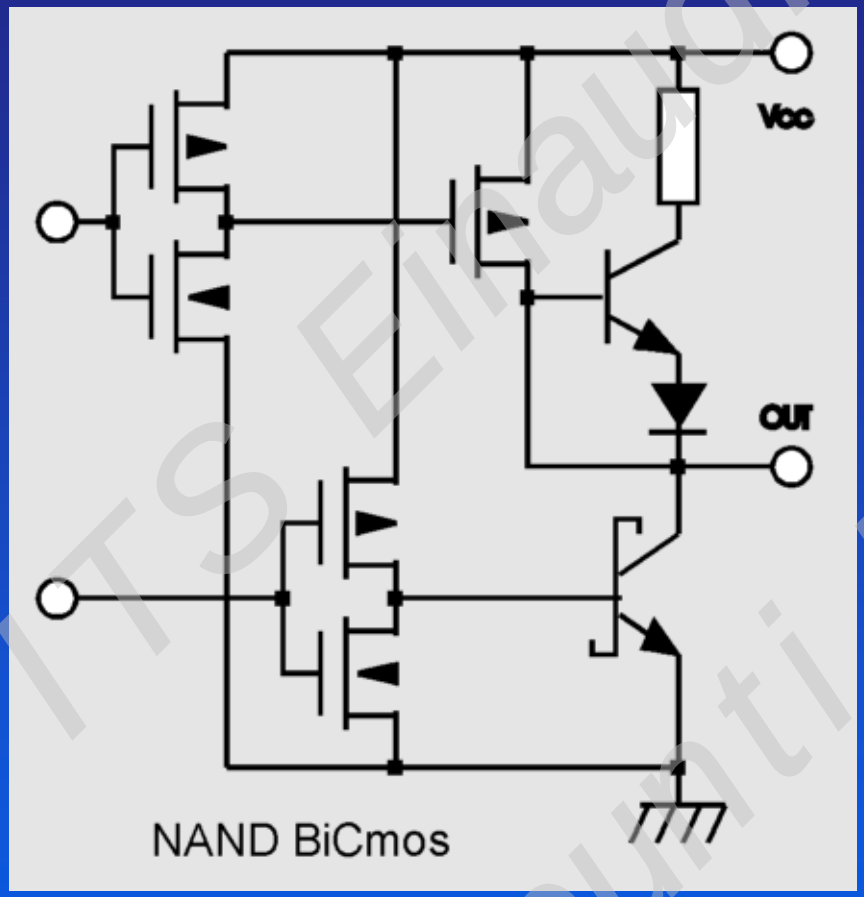


NAND e NOR CMOS





PORTE LOGICHE - logiche BiCmos



NAND BiCmos

ITS Einaudi Appunti T.D.P.

PORTE LOGICHE - varie famiglie

LOGICHE STANDARD

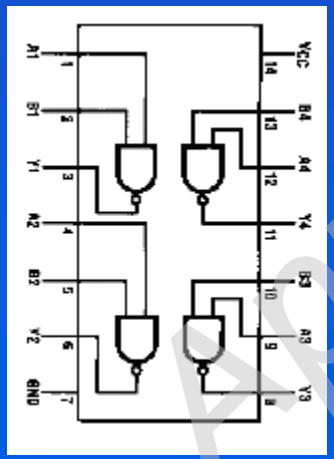
LOGICHE TTL (bipolari)

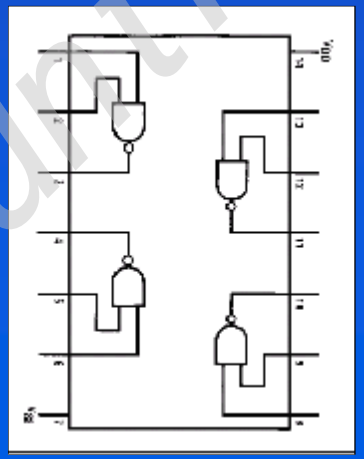
- 7400	TTL
- 74S00	Schottky -TTL
- 74F00	Fast – TTL
- 74LS00	Low-Power S -TTL
- 74AS00	Advanced S -TTL
- 74ALS00	Advanced LS -TTL

LOGICHE CMOS

- 4000	CMOS classiche
- 74HC00	High-Speed Cmos pin-compatibile TTL
-74HCT00	High-Speed Cmos pin-compatibile TTL level-compatible TTL
-74ACT00	Advanced CMOS

7400 TTL





4011 Cmos

PORTE LOGICHE - un confronto

parametro	74xx	74LS	4000	74HCT	unità
Vcc nominale	5±10%	5±5%	3...15	2…6	V
Vcc massima	8	5.5	20	7	V
Pd/gate typ-	10	8	10^{-3}	10^{-2}	mW
Fan Out	10	10	50	10	- -
tpd typ	10	5	60	8	nsec
freq. massima	20	40	5	30	MHz
V_{IH} (minima)	2	2	V_{DD} –30%	2	V
V_{IL} (massima)	0.8	0.8	30% V_{DD}	0.8	V
V_{OH} (minima)	2.4	2.7	V_{DD}	4.9	V
V_{OL} (massima)	0.4	0.5	0.05	0.1	V
I_{IH} massima	0.1	0.1	10^{-6}	10^{-4}	mA
I_{IL} massima	-1.6	-0.4	-10^{-6}	-10^{-4}	mA
I_{OSC} massima	-55	-100	-2	-40	mA

PORTE LOGICHE - l'evoluzione

1960: logiche RTL (Resistor-Transistor Logic)

1965: logiche DTL (Diode-Transistor Logic)

1970: logiche TTL (Transistor-Transistor Logic)

1972: logiche HLL (High-Level Logic)

1975: logiche CMOS (Complementary Metal-Oxyde Semiconductor)

1980: logiche Schottky (S-TTL, AS, LS, FAST)

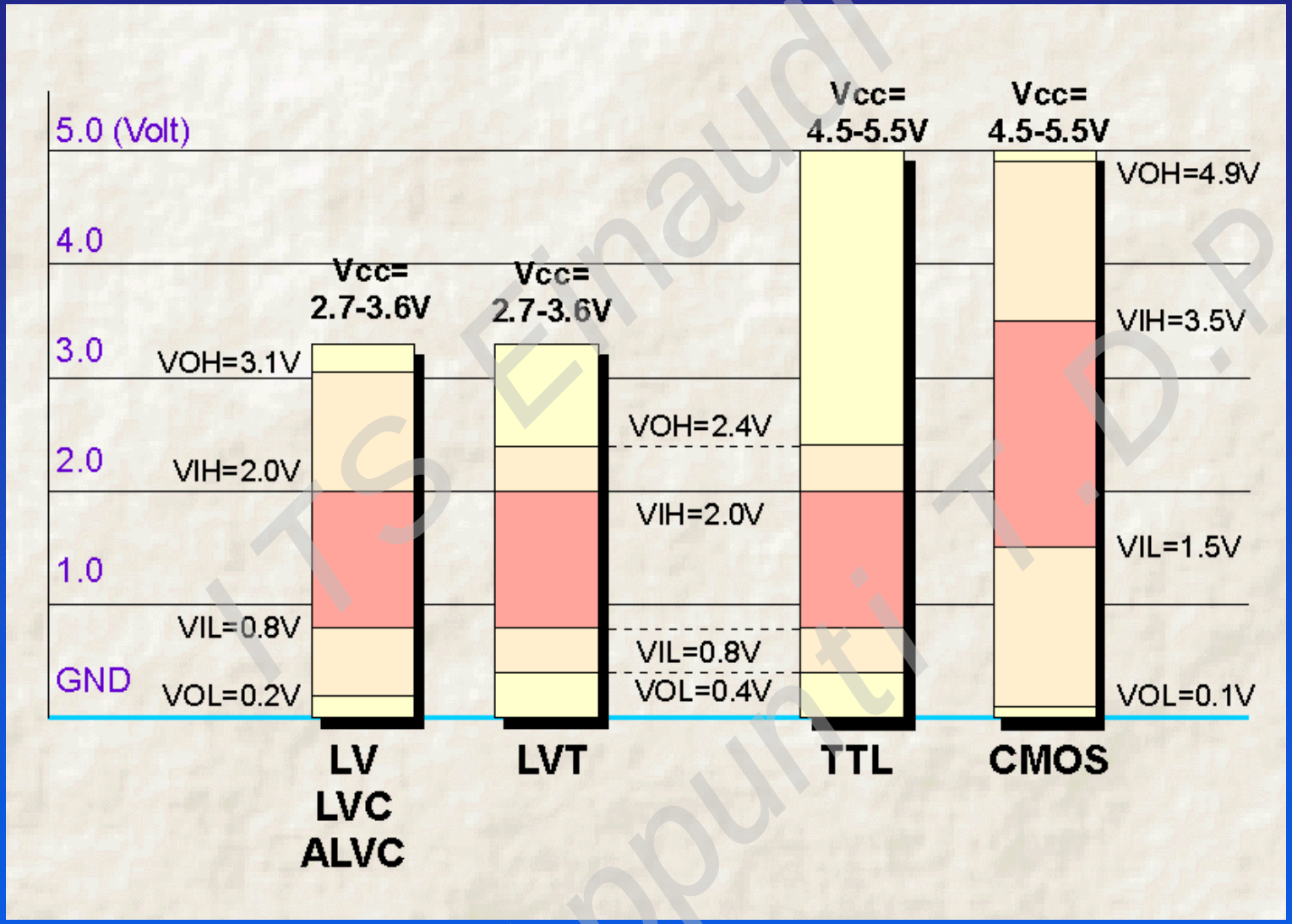
1990: logiche HCmos (High-Speed Cmos Logic)

1995: logiche BiCmos (Bipolar & Cmos Logic)

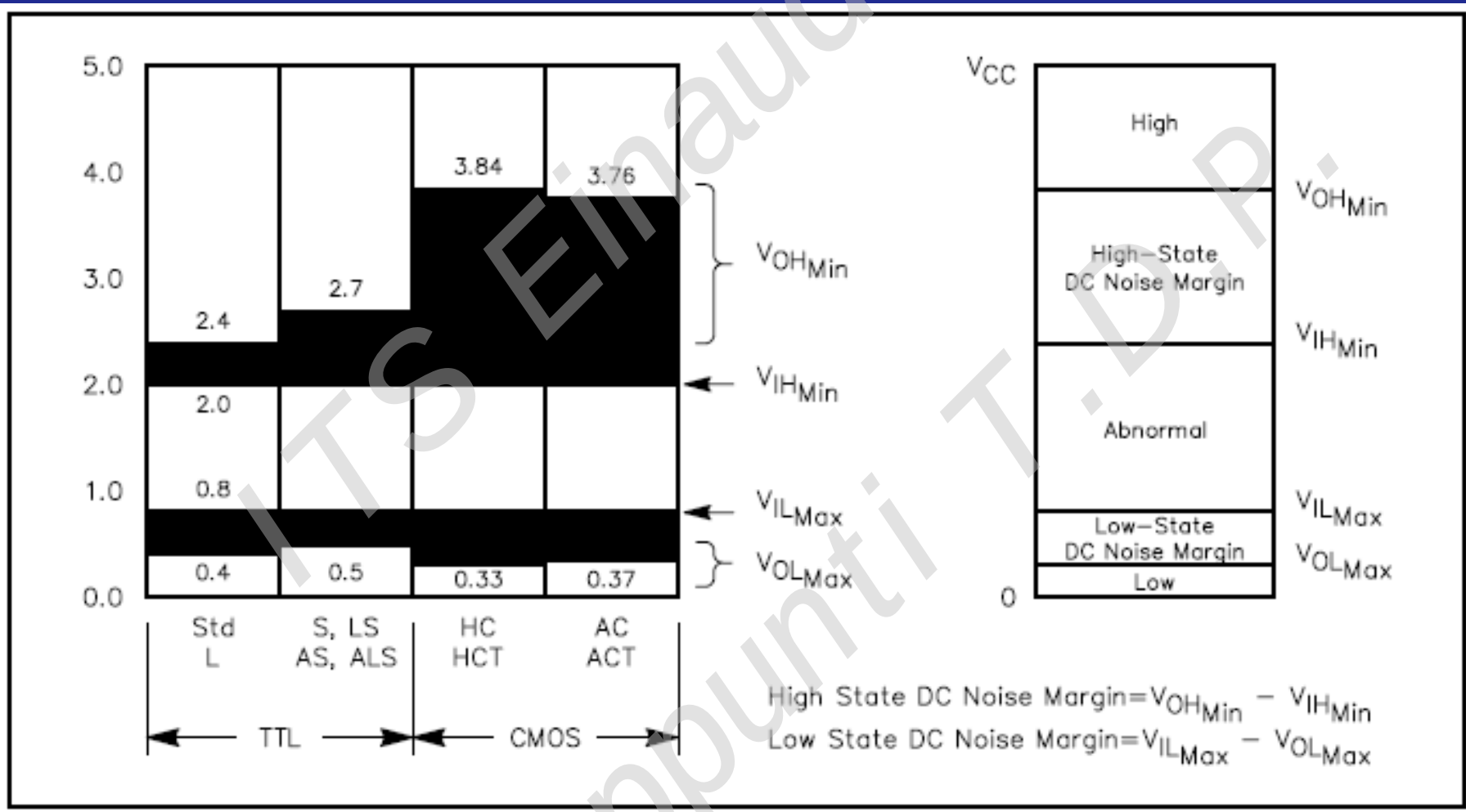
Parametri-chiave:

- **velocità (tpd)**
- **tempi di salita/discesa (tf, tr)**
- **dissipazione (Pd/gate)**
- **fan-out**
- **tensione di alimentazione**
- **integrabilità**

PORTE LOGICHE - i livelli logici



PORTE LOGICHE - Interfacciamenti



PORTE LOGICHE - Interfacciamenti

Interfacciamento garantito se:

a) Uscita del dispositivo pilotante al livello alto :

$$V_{OHMIN} > V_{IHMIN} \qquad |I_{OHM}| > |I_{IHM}|$$

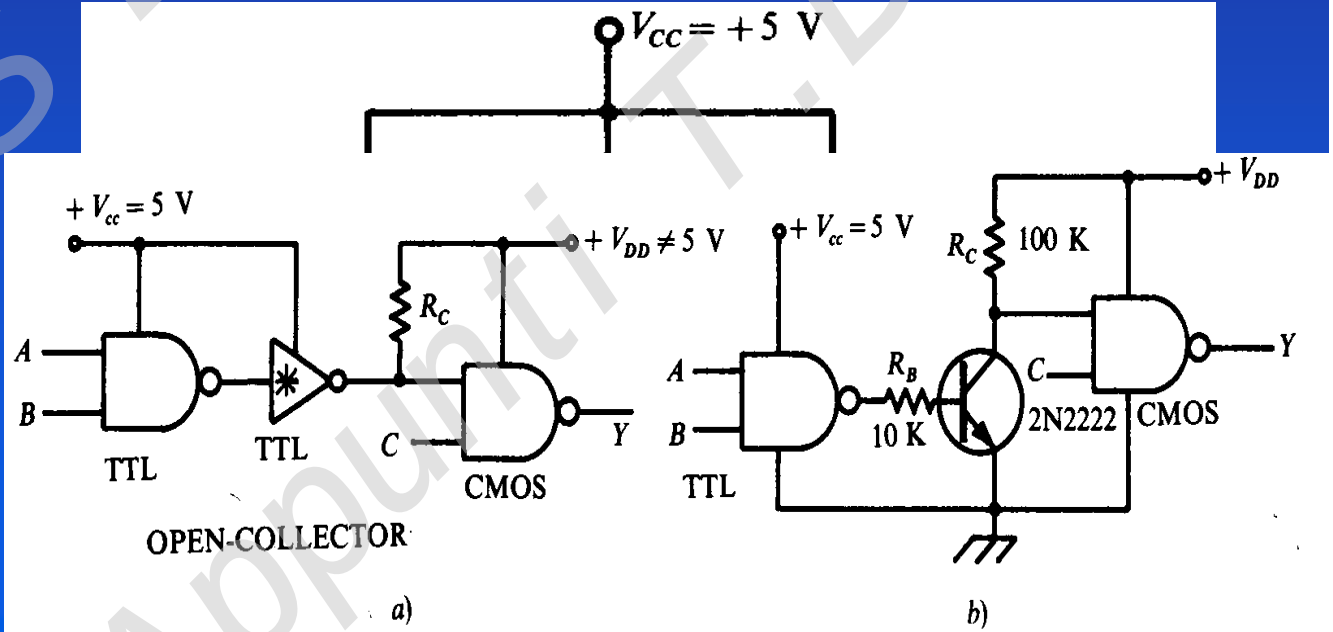
b) Uscita del dispositivo pilotante al livello basso :

$$V_{OLM} < V_{ILM} \qquad |I_{OLM}| > |I_{ILM}|$$

TTL che pilota CMOS

con diverse alimentazioni

$$Rc \geq \frac{Vcc - V_{OLM}}{I_{OL}}$$



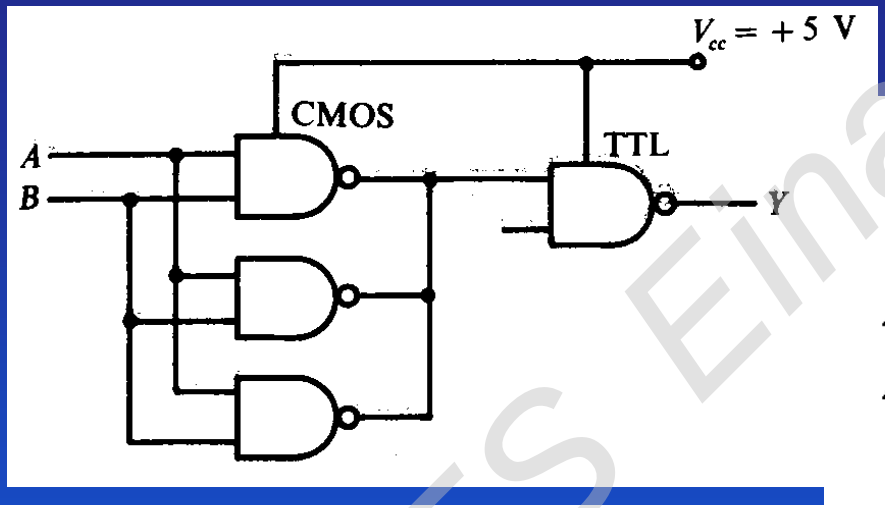
a) Interfacciamento tra un dispositivo TTL open-collector e uno CMOS nel caso di alimentazioni diverse

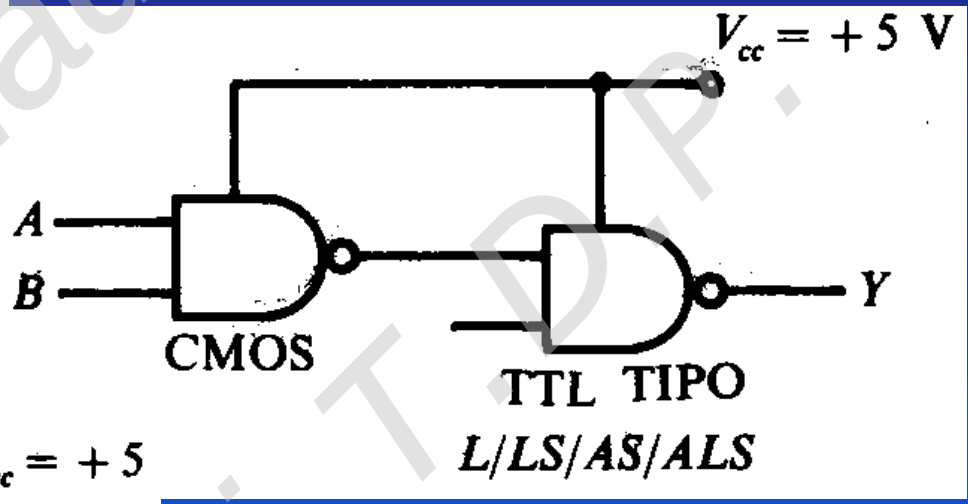
b) schema con BJT

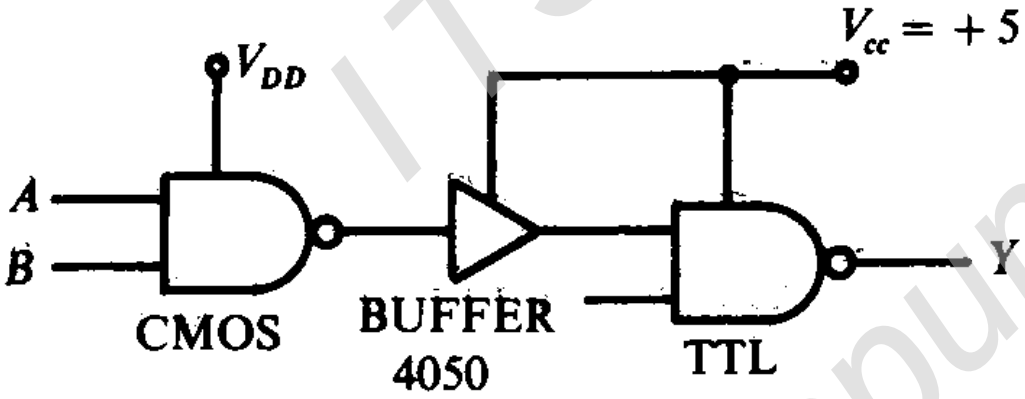
PORTE LOGICHE - Interfacciamenti

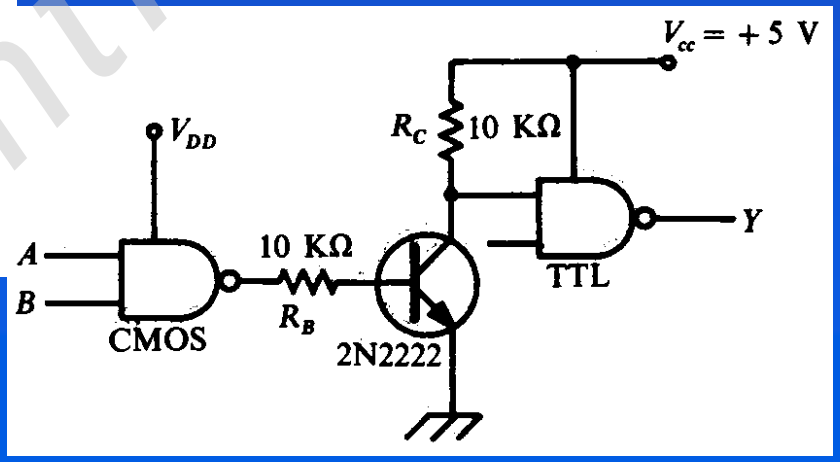
CMOS che pilota TTL

Problematiche non sui livelli di tensione ma sulle correnti a livello basso

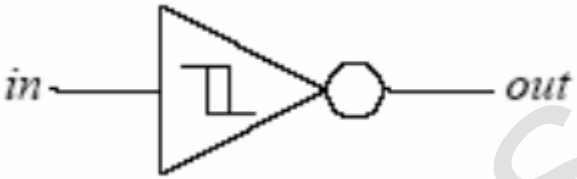


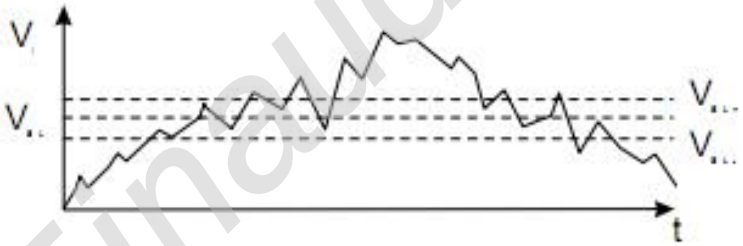


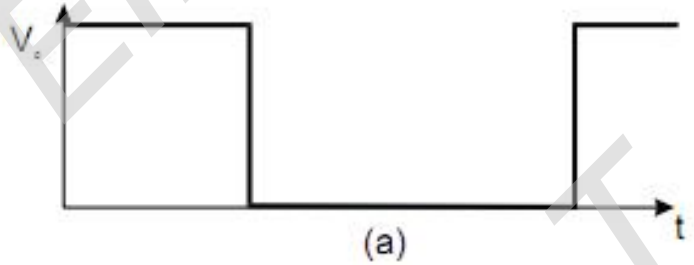




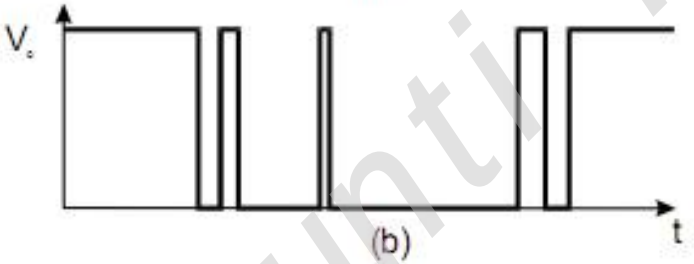
Invertitore con isteresi (trigger di Schmitt)







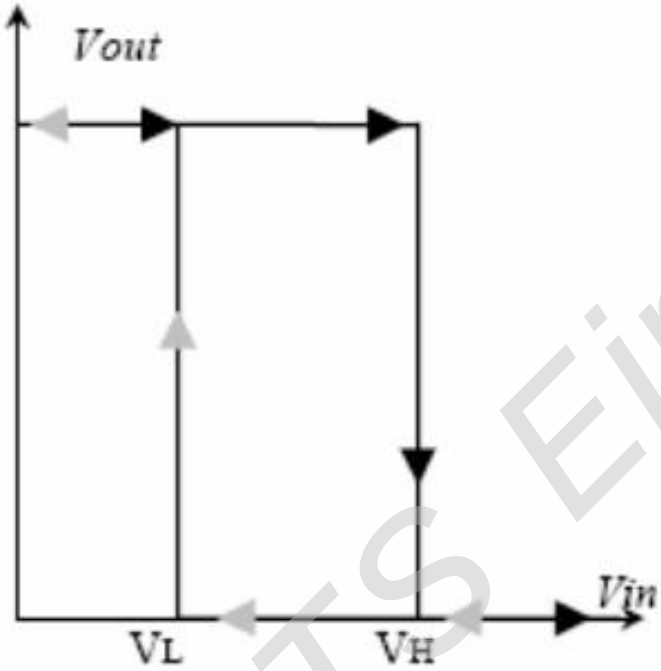
(a)

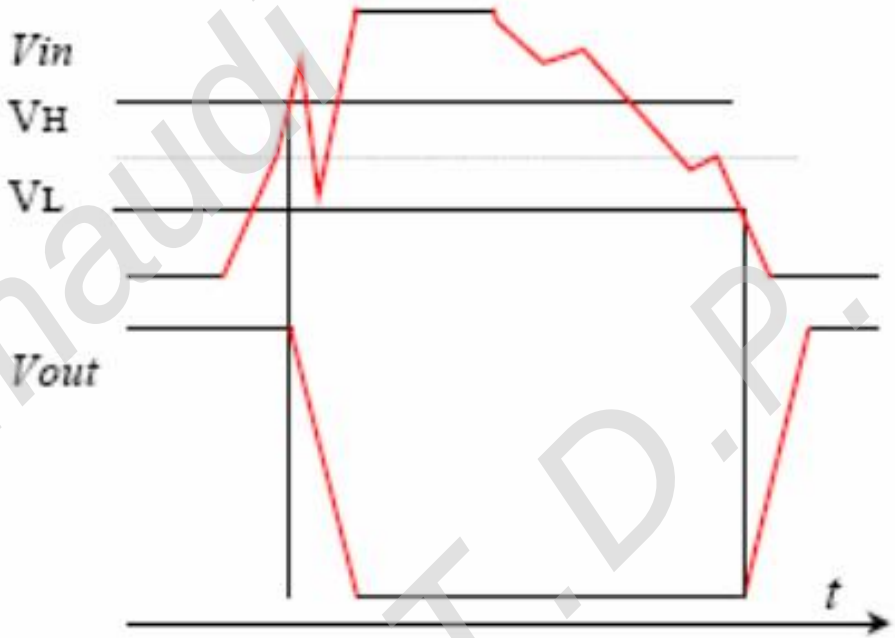


(b)

a) Risposta di un invertitore con isteresi

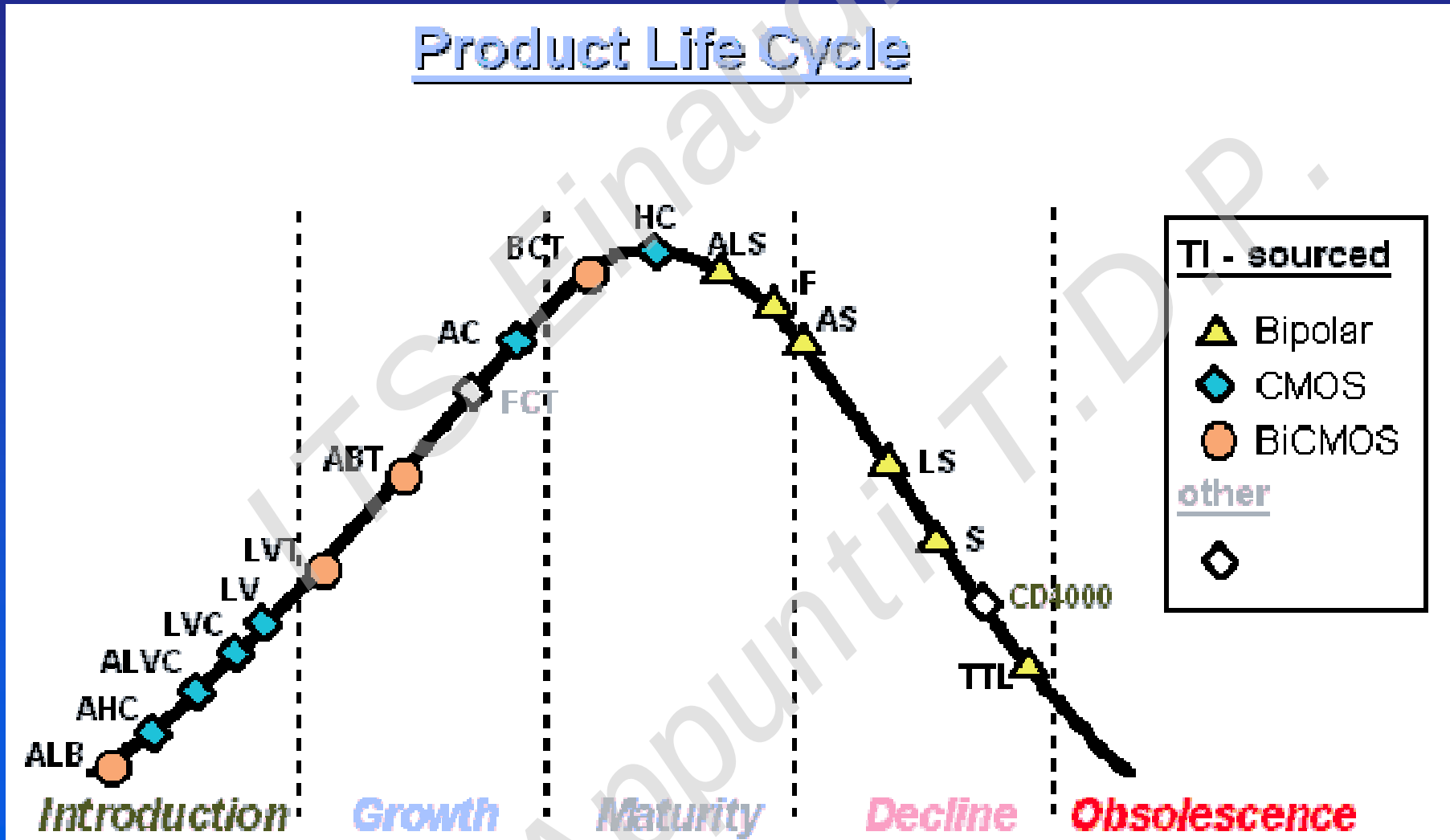
b) Risposta di un invertitore semplice → **commutazioni multiple**



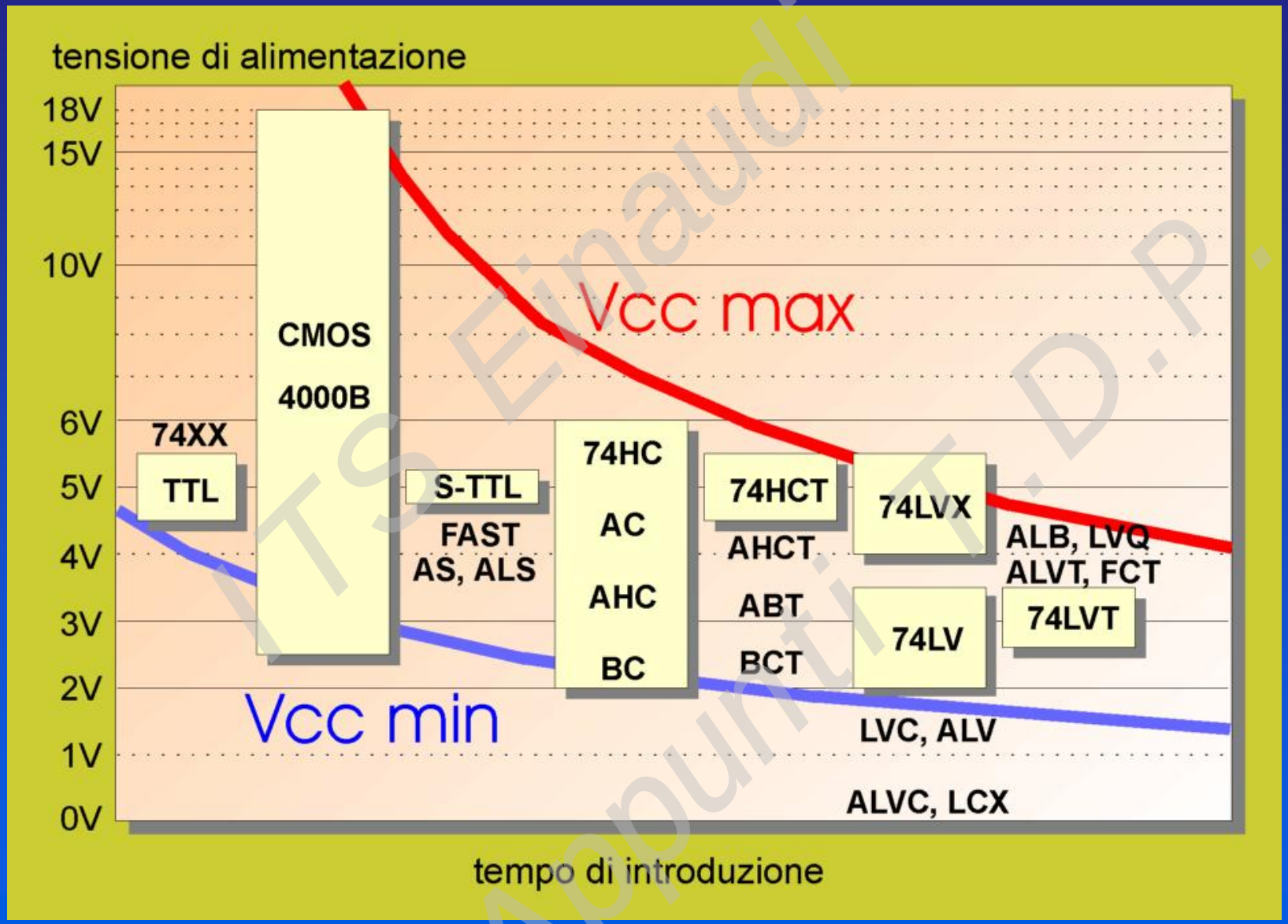


- Differenti soglie sul fronte di salita e sul fronte di discesa
- Soglie funzione dei parametri circuitali e di V_{DD}
- A livello elettrico, non è, a rigore, una porta combinatoria

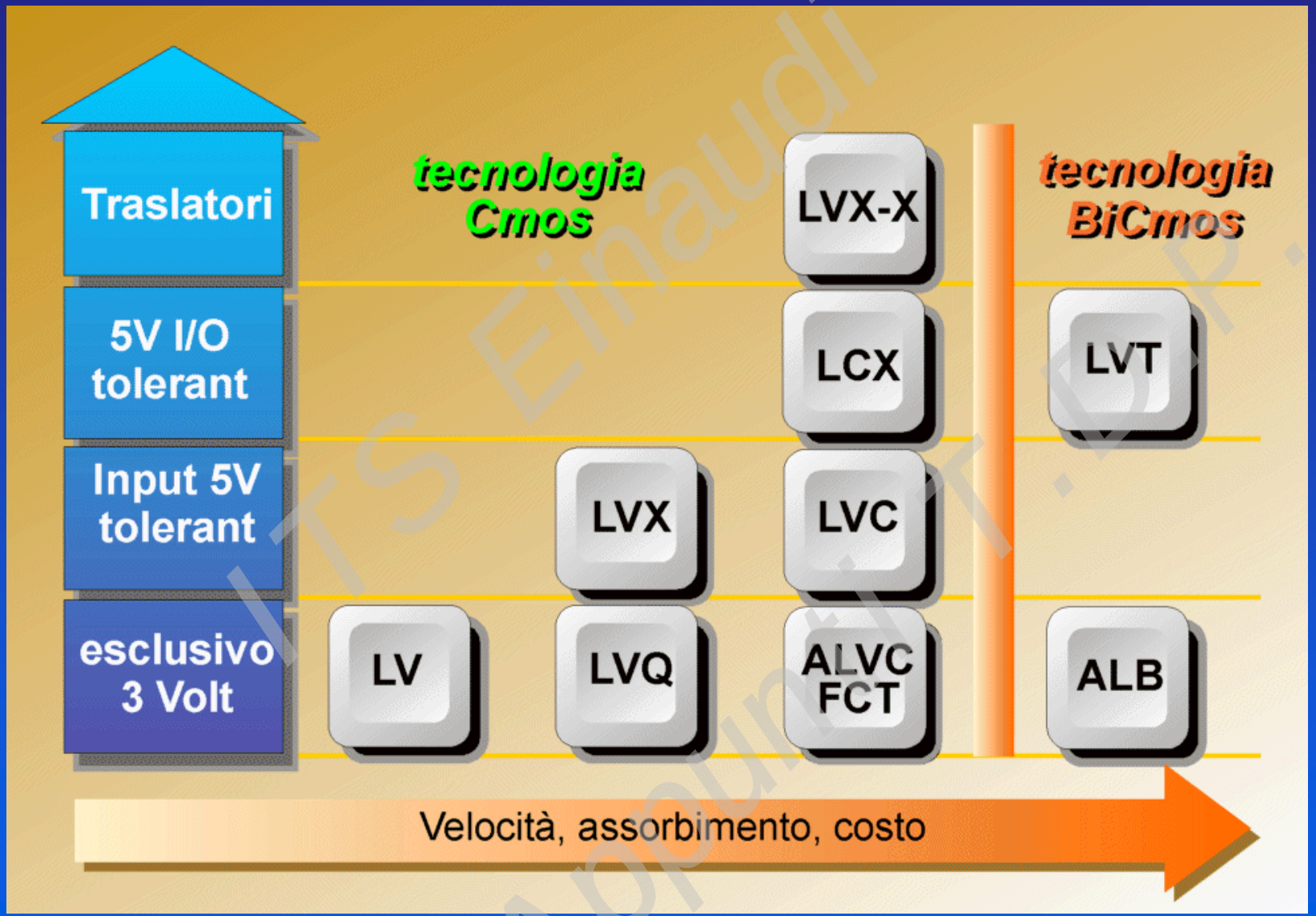
Stato attuale delle famiglie logiche nel ciclo di vita



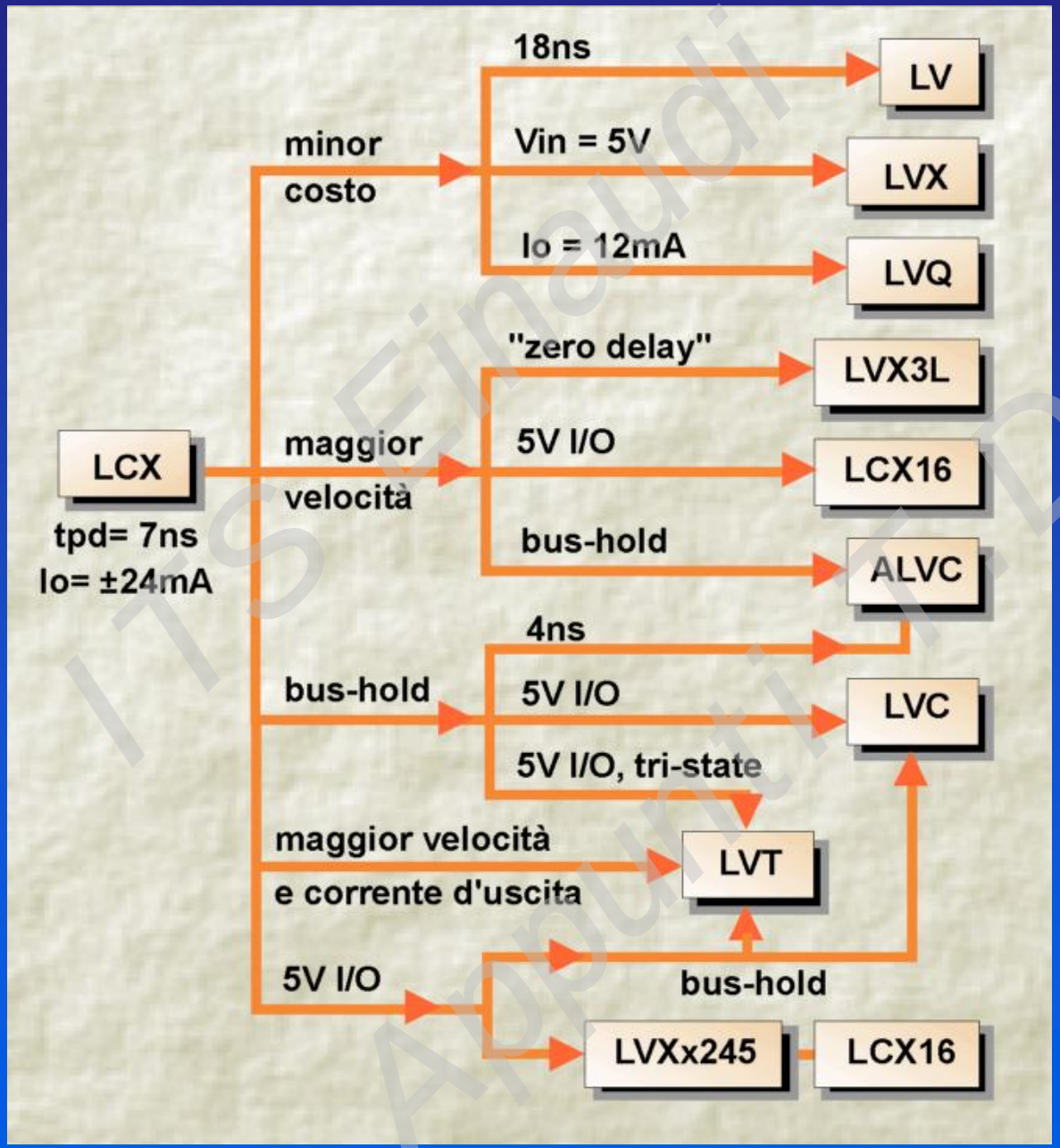
PORTE LOGICHE - tensione di alimentazione



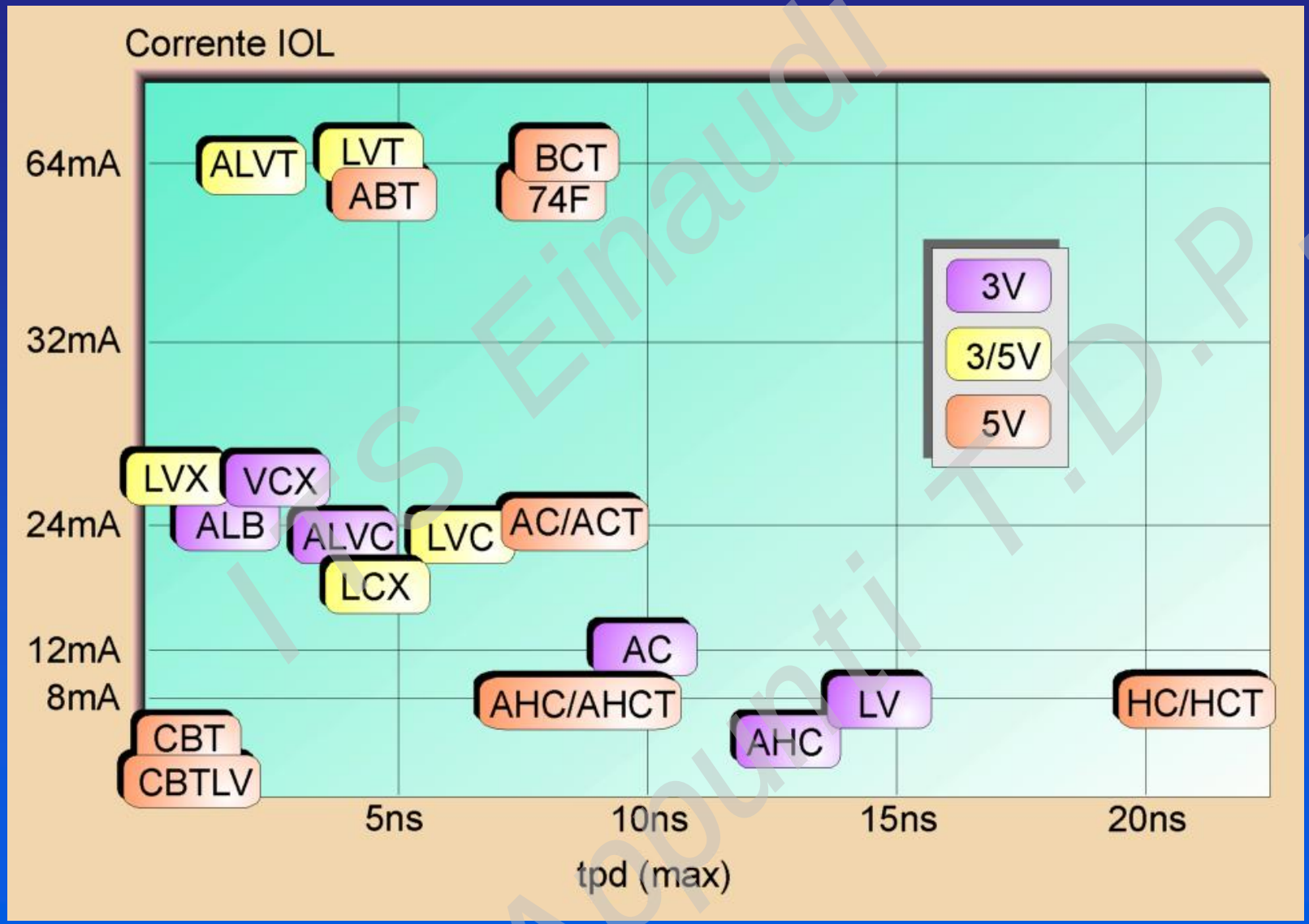
PORTE LOGICHE - specializzazione



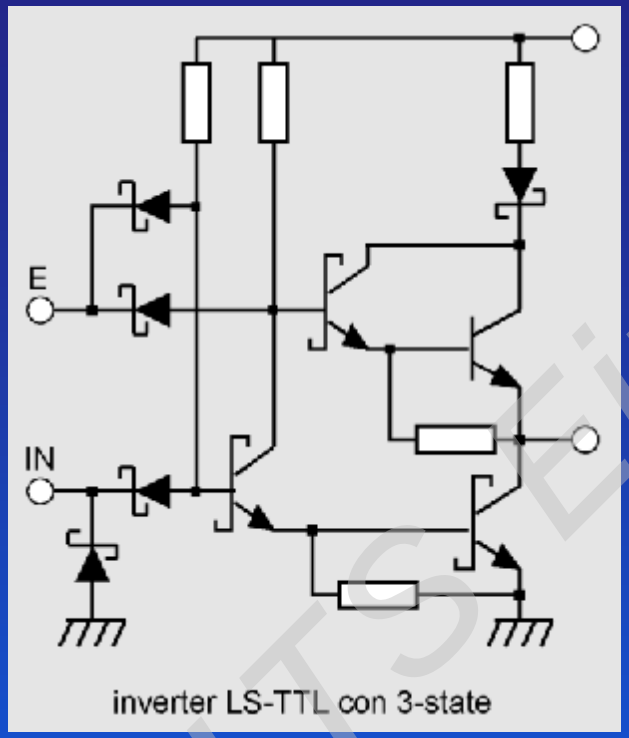
PORTE LOGICHE - esigenze applicative



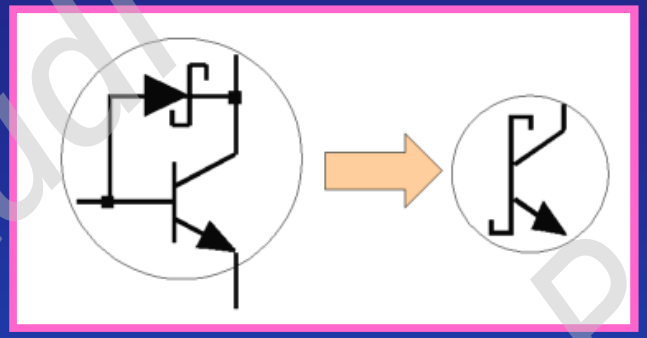
PORTE LOGICHE - corrente d'uscita/velocità

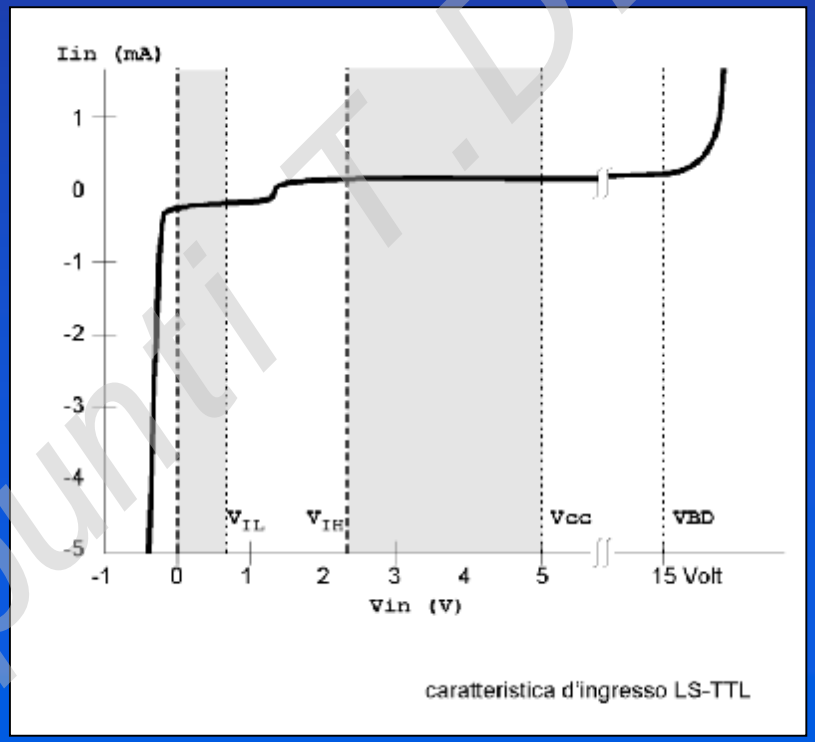


PORTE LOGICHE - Schottky-TTL



inverter LS-TTL con 3-state





caratteristica d'ingresso LS-TTL

PORTE LOGICHE - Schottky - TTL - Cmos